63-2-3

PRODUCTION ENGINEERING MEASURE

2N1358A TRANSISTOR

QUARTERLY PROGRESS REPORT NO. 2
FOR THE PERIOD
JULY 30, 1962 TO OCTOBER 30, 1962

CONTRACT NO. DA-36-039-SC 86725
ORDER NO. 19047-PP-62-81-81

PLACED BY

U. S. ARMY ELECTRONICS MATERIEL AGENCY
PHILADELPHIA, PENNSYLVANIA

solid state
electronics

DELCO RADIO
DEPENDABILITY RELIABILITY

General Motors Corporation
Kokomo, Indiana

COPY NO. 11

PRODUCTION ENGINEERING MEASURE TO IMPROVE PRODUCTION TECHNIQUES AND INCREASE THE RELIABILITY OF THE 2N1358A TRANSISTOR

QUARTERLY PROGRESS REPORT NO. 2 FOR THE PERIOD JULY 30, 1962 TO OCTOBER 30, 1962

OBJECT:

To modify production equipment to incorporate improved techniques and perform the necessary tests to demonstrate the capability of the improved production line.

CONTRACT NO. DA-36-039-SC 86725
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PREPARED BY: J.C. KUHNS
APPROVED BY: K.W. DOVERSBERGER

DELCO RADIO

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DELCO RADIO

1.0 ABSTRACT

This report is a review of the work during the second quarter, July 30, 1962, to October 30, 1962, of the contract. During this quarter, the first quarterly report was submitted, reviewed, approved, and distributed. The third engineering sample group of transistors was submitted.

Of the 17 planned equipment and process modifications, 3 are in effect and being used as standard production. In addition to the originally planned activities, a considerable amount of effort is being directed toward solving the particular causes of reliability type failures. Detailed reports of this work are included in this report. Critical path planning was altered to include these programs and attempt to finish them within the contract time period.

During the second quarter, information from the reliability testing program was accumulated and analyzed. The Milestone I test completed 1000 hours on test and the results are tabulated and included in this report. Also, relationships between the daily manufacturing tests, accelerated life tests, and special step-stess tests are being developed. It is anticipated that greatly accelerated tests will enable time to be saved on process evaluation tests.

The failure analysis program has continued to yield information as to the nature of failures and provides a quantitative measurement of the various failure modes.

In the analytical-empirical surface study program, numerous experiments have been run and analyzed. It is hoped that the means of achieving parameter stability can be derived from this program.

2.0 PURPOSE

The purpose of this program is to improve the reliability of the 2N1358A transistor by specific improvements of manufacturing techniques. The program plan includes equipment and process modifications, a reliability test program, a failure analysis program, and an analytical-empirical surface study program.

In the endeavor to reach the failure rate objective, the following processes are to be improved:

1. Crystal Growing
2. Crystal Slicing
3. Automatic Scribe
4. Wafer Etching
5. Solders and Indium Separation
6. Collector Disc Etch
7. Wafer Flash Etch
8. Alloy Boat Assembly
9. Unitron Microscope
10. Alloy Boats
11. Alloy Furnace
12. Base Preparation Furnace
13. Mount Furnace
14. Automatic Test Set (Capper)
15. Continuous Cap Wash
16. Cap Date Coder and Pin Insulator Press
17. Manufacturing Building

Additionally, the program includes preparation and submission of engineering samples, quarterly reports, a final engineering report, bill of material and parts, and a general report on Step II (twice the maximum rate attainable with existing facilities).

3.0 PROGRAM PROGRESS

Progress on the program is reported in this section under the headings of "Equipment and Process Modifications," "Reliability Testing," "Failure Analysis," and "Analytical-Empirical Surface Study."

3.1 EQUIPMENT AND PROCESS MODIFICATIONS.

Of the 17 modifications specified in the contract, three were effected into production during the first quarter, and none were completed during the second quarter. However, progress has been made and the third quarter should see the culmination of a number of the programs. Relating to the processes, a large amount of work has been done on the problems causing reliability type failures. Reports on this work are included in this section.

3.1.1 Germanium Crystal Growing - H. G. Dohmen.

General. The objective of the crystal growing effort is to improve the germanium crystal quality by elimination of grain boundaries, reduced etch-pits, and finer resistivity control. To achieve this, various techniques have been tried with both horizontal and vertical type growers.

Engineering Status. The difficulties with the resistance furnace burn-out on the experimental horizontal grower were corrected with platinum resistance wire. This equipment is now capable of producing crystal well within the resistivity range required and with etch-pit counts averaging below 3000/cm^2.

Work with constant pull rates on the vertical growers was not fruitful quality-wise. No detectable differences were discernable in the crystals produced versus standard production.

On unit size crystals, the efforts to control the diameter variations (crystal to crystal) were successful. This was done by equipping the T. V. camera with a 6 inch lens providing approximately 30X magnification. The diameter is then controlled by maintaining the molten zone within a fixed number of horizontal scanning lines on the raster. Height control of the molten zone within ± 18% is providing diameter control within ± 2. 8% which is within the product design specifications. Indications are the height can be controlled within ± 8%.

The relative merits of the various growing techniques were reviewed and the basic decision has been made to pursue the unit size crystal growing technique. This decision was predicated on both quality and economic factors. The evidence is lifetime and can be held>50μsec., resistivity within 1 Ωcm, the maximum etch-pit count should be< 8000/cm², and the crystal will be free of grain boundaries. Accordingly, critical path plans have been made for the acquisition of a production prototype machine and conversion of production to unit size growing. Management authorization to proceed with the production prototype has been granted, and an appropriation request for the complete conversion is being prepared.

Quotations for the prototype and peripheral equipment have been received and orders for the monitoring and diameter control equipment have been let.

Conclusions. The basic conclusion reached in this quarter is that unit size crystal growing provides the best means of supplying high quality crystal economically under production conditions.

Program for the Next Quarter. The program for the next quarter is to verify, by a field trip, potential suppliers' capabilities; order the prototype grower and supplemental equipment, and obtain the appropriation for the complete conversion.

3.1.2 Crystal Slicing - W. H. Keisling.

General. The germanium crystal slicing operation is being changed from O. D. (outside diameter) to I. D. (inside diameter) saws. The I. D. sawing provides better directional control of the cutting plane, reduced taper on the slices, and improved orientation. Also, the I. D. blades are thinner and have finer grit diamonds, so there is less crystal surface damage and less kerf loss.

Engineering Status. At the time the PEM program started, there were three machines - two Do-All and one Brown and Sharpe - to be converted to I. D. saws. To date, one Do-All and the Brown and Sharpe have been converted, and the remaining machine is being returned to the factory for conversion. The Production Department is now slicing exclusively on I. D. saws.

Conclusions. The internal sawing capacity is now adequate to fulfill all slicing requirements.

Program for the Next Quarter. The remaining saw will be returned during the next quarter, and the program will be completed.

3.1.3 Automatic Scribe - J. C. Kuhns.

General. The present semi-automated scribe, with a carbide tool, produes a small percentage of wafers with chipped corners and uneven scribe lines. The proposed machine will have diamond tools which should reduce uneven breaking and chipped corners. Dimensional control of the wafers will be better with the new machine. This will enable improvements of the relative location of the wafer and base ring assembly.

Engineering Status. In view of the apparently successful development of unit size crystal growing techniques which would obsolete the need of scribing equipment, this program has been held in abeyance during the 2nd Quarter.

Conclusions. None.

Program for the Next Quarter. Because of success with the unit size crystal growing program and management authorization to proceed, it is planned to request a substitute for the automatic scribe program.

3.1.4 Wafer Etch - J. F. Norwich.

General. Presently, germanium wafers are etched manually (hand transfers in baskets between solutions) to remove the disturbed layer caused by slicing and to reduce the wafer thickness to the desired dimension. The plan is to mechanize the operation and improve other aspects.

Engineering Status. In the last report, it was pointed out that incompatibility exists between machine transfer times and the time elements of the process. To resolve this dilemma, a study of the mechanics and chemical reactions of our process is in progress. The object is to revise the process maintaining the necessary consistency for reproducibility of the product and to achieve a uniform transfer time within machine capabilities.

Conclusions. To fulfill this mechanization program, a change in process is required, but the degree of change is not yet evident.

Program for the Next Quarter. The plan is to continue the present analysis to enable the design to be finished.

3.1.5 Solder and Indium Separation - L. E. Lower.

General. The possibility exists, at present, of cross-contamination between solders and indium alloys, resulting from sharing basic equipment, although separate tooling. To eliminate this possibility, duplicate equipment will be provided in separate rooms in the new Manufacturing Building.

Engineering Status. The move into the new Manufacturing Building has not progressed as rapidly as originally intended with the result this program did not get completed in the 2nd Quarter. However, the die, safety shield, and take-up reel were installed on the new extrusion press, and the debugging of this equipment is nearly completed. Also, the refrigeration equipment used in conjunction with the indium mix furnace is ready for operation.

Conclusions. There are no appreciable technical problems expected in completion of this program. It is now simply a matter of scheduling the balance of relocation and installation work to be done.

Program for the Next Quarter. It is planned to complete the installation of all of the equipment and commence operation in the next quarter.

3.1.6 Collector Disc Etch - J. F. Norwich.

General. There has been evidence that the present etching process on the collector discs (indium alloy) helps create an undesirable oxide layer on the disc. The program is to eliminate the etching operation.

Engineering Status. The data on the first sample groups produced with unetched collector discs, indicates a grave degradation on modulation life test (23% failure rate). Also, unwet

area counts of emitters produced without the etching show an increase. This is not true for collectors, probably because the alloy process on collectors is more tolerant, but it tends to indicate elimination of the etching operation is not actually a quality improving factor. To verify this information, another complete set of experiments have been produced over three different production days. The units from these experiments are now being environmental tested.

Conclusions. Successful completion of this program is in doubt.

Program for the Next Quarter. The program for the next quarter is to complete the evaluation of the efforts to date, and on that basis procede with the program or seek a substitute program with more favorable reliability features.

3.1.7 Wafer Flash Etch - L. E. Lower.

General. Germanium wafers are given a flash etch for cleaning purposes prior to the alloying operation. This program was to provide equipment to enable the flash etch to be performed in the alloy area and reduce the elapsed time between the two operations. The program has been completed.

3.1.8 Alloy Boat Assembly - G. E. Dieterly.

General. The assembly of the wafer, emitter and collector preforms, base ring, and center base contact into alloying boats is

done in room air. Airborne contaiminants, such as dust, could settle on the parts and cause small imperfections. The plan is to enclose the furnace assembly table in a dust-free cabinet.

Engineering Status. Although the equipment is available to complete this program, the need for the dust cabinets in the environment of the new Manufacturing Building is unknown. The move of the alloy department is in progress, and should be completed in two weeks. When the move is completed, a study will be made to determine the effectiveness of the cabinets.

Conclusions. At this time, no qualified statement can be made about the usefulness of dust shields in the alloy area.

Program for the Next Quarter. During the next quarter, a study of the dust condition in the area (electrostatically filtered air) will be made. It is planned to setup the shield in the area, to make comparative dust counts. On the basis of this study, the next steps will be determined.

3.1.9 Unitron Microscope - G. E. Dieterly.

General. This program is to supply an additional inspection tool (microscope) to insure proper construction and maintenance of the graphite alloying tools. The microscope will supplement the air gages and comparator already used for this purpose.

Engineering Status. The appropriation to buy this equipment was approved. The microscope was ordered and has been received. It has not yet been put to scheduled use.

Conclusions. The microscope will be a valuable addition to the alloy boat inspection program, and possibilities do exist for additional valuable applications, possibly as a measuring tool to enable better control of the diode etching operation.

Program for the Next Quarter. The microscope will be installed and personnel trained in its proper use.

3.1.10 Alloy Boat - G. E. Dieterly.

General. The feasibility of a new alloy boat designed to produce more planar emitter junctions (comparable to the collector junction) has been demonstrated in a laboratory. The program is to reduce the laboratory method to production practice on the 2N1358 type transistor element.

Engineering Status. One alloy boat has been made and tried several times using a converted production furnace. At present, the results with this boat are being studied from a production standpoint for its ability to make good planar transistor elements, and to assess the durability and maintenance requirements of the boat. Additional runs are being made. An appropriation request for an adequate quantity of production boats has been submitted.

Conclusions. An acceptable boat design can be finished by January 1, 1963.

Program for the Next Quarter. A final decision on boat design will be made during this quarter. The appropriation should be approved and construction started on production quantities.

3.1.11 Alloy Furnace - G. E. Dieterly.

General. In conjunction with the proposed alloy boat change (Paragraph 3.1.10), modifications of the alloy furnace are needed for both mechanical reasons and an optimum alloy curve (time versus temperature).

Engineering Status. A production alloy furnace has been converted to run the new type alloy boat. Furnace conveyors have been completed. Work on setting the optimum alloy curve is in progress. Studies of the effects of the furnace time and temperature characteristics as they affect the generation of spur regrowths have been made (Paragraph 3.1.19).

Conclusions. None

Program for the Next Quarter. An effort will be made to determine the optimum alloy curve by December 1, 1962, and any additional conversion needed to the furnace will be made the

following month. Additional trial runs with the hydrokinetic boat will be made. Work layout will be studied and design of mechanical stations completed.

3.1.12 Base Preparation Furnace - R. N. Goings.

General. The base preparation operation consists of soldering two terminal assemblies to the nickel plated copper base and pretinning the pedestal on the base. The previous method for this operation was to use rosin flux and solder the assembly in a furnace. The flux was then removed in a series of trichoroethylene baths. The program was to perform the same operations in a hydrogen atmosphere, eliminating the flux and associated contaminants.

Engineering Status. The hydrogen base preparation furnace has been in production during the 2nd quarter of the contract.

Conclusions. The hydrogen base preparation is working in a satisfactory manner.

Program for the Next Quarter. Because of the possibility of combining this operation with the mounting operation, an investigation of this possibility is continuing.

3.1.13 Mount Furnace - R. N. Goings.

General. The mounting operation consists of mounting the transistor elements to the base and connecting the base and emitter

contacts to the terminals. The mounting is done in a furnace with a hydrogen atmosphere. The plan is to develop a furnace with superheated hydrogen for superior fluxing action. And now, if possible, it is planned to combine the base preparation operation (3. 1. 12) with the mounting.

Engineering Status. The new furnace has been installed, and development of a process to combine operations has been started. Initially, there was some difficulty with moisture getting into the system causing some discoloration on the solders. The plumbing leaks causing this have been found and corrected, and an acceptable dew point is now being maintained. At present, a good mounting job is being achieved, but there is about a 10% loss due to solder bridging across the glass seal on the terminals. Corrective means are limited because of incompatibility of the various solders involved. However, the problem is being attacked through various furnace control means, volume control of the terminal solder, and the staking configuration on the terminals.

Conclusions. Although there are still some problems, the program looks good. There is less difficulty with emitter indium dewetting than with the standard production operation.

Program for the Next Quarter. The process development work will continue and sample units will be submitted for engineering evaluation.

3.1.14 Automatic Test Set (Capper) - H. E. Wright.

General. The purpose of this project is to reduce damage to the transistors by eliminating handling at the test after mount station. This will be accomplished by testing the transistors automatically rather than manually. In addition to performing the go - no go tests on the diodes and gain, a parameter distribution of these three parameters will be made. This distribution will aid in analyzing troubles in the preceding processes.

Engineering Status. A cost estimate of $12, 600 was completed and the appropriation was obtained.. All major parts have been ordered and many have been received. Construction has not been started since the final drawings have not been completed.

Conclusions. Some difficulty has been experienced in the design of (1) the test jig used to apply the test signal, and (2) the memory device that will prevent capping of rejected units. It had been planned to use a test jig similar to a previous application, but this did not prove possible. Also, the problem of remembering the results of the test are slightly different on this problem than it was on prior application so that a more complicated memory system had to be devised. This new design has been agreed upon, but the final mechanical drawings have not been made.

Program for the Next Quarter. During the next quarter, the drawings will be completed, all parts will have been received and the necessary modifications made, and construction completed.

Assuming no changes in the basic specifications, there should be no major problem in placing the set into production.

3.1.15 Continuous Cap Wash - R. N. Goings.

General. At present, the cap washing facilities are in a different department than the capping press. The caps are washed and then stored for varying lengths of time before usage. The new cap washing will be directly on the capping line reducing the chance of contamination before use. This system will include a baking operation to insure dry caps.

Engineering Status. This equipment has been debugged and is ready for installation when the assembly line is moved to the new Manufacturing Building. There have been cap feeding troubles in the vibrating accumulator.

Conclusions. None

Program for the Next Quarter. Relocation of the final assembly line will be made, and the cap washing equipment will be installed.

3.1.16 Cap Date Coder and Pin Insulator Press - F. R. Gustin.

General. Transistor caps are date coded on an automatic marking machine prior to assembly on the transistors. The possibility of

cap contamination exists. Nylon insulators are assembled to the locator pin, when required, with an arbor press. Handling damage can occur. This program is to provide an automatic machine in line with the capping press to perform both the coding and the insulator assembly.

Engineering Status. Mechanical construction of the machine has been completed and the electrical wiring is 50% done. It appears that the total construction can be completed by November 15, 1962.

Conclusions. None

Program for the Next Quarter. During the next quarter, the machine construction will be completed, and it is hoped the debugging and installation can be completed.

3.1.17 Manufacturing Building - G. M. Wagner.

General. Manufacturing of semiconductors has been in an old building that is difficult to keep clean enough to assure satisfactory conditions for the manufacture of reliable transistors. The new Manufacturing Building has been designed specifically for semiconductor work. It has many features to provide proper atmospheric and environmental conditions.

Engineering Status. At the present time, all germanium transistor activities have been transferred, or are in the process of

being transferrred to the new Manufacturing Building, except for the final assembly lines. The move has proceeded slightly slower than anticipated because of complications in maintaining production during the move.

Conclusions. Relocation of facilities without disruption of production has been complicated, but is being accomplished.

Program for the Next Quarter. The final assembly lines will be moved during the next quarter, enabling more concentration on the other items in the program.

3.1.18 Diode Degradation - M. E. Stanton.

General. Early in the PEM Program, failure analysis results made it rather obvious that to meet the failure rate goals of the contract, positive action would have to be taken in production to correct, or at least alleviate, the condition contributing to collector diode degradation. Although a number of the proposed production changes could influence the condition; notably the new alloy boat, hydrogen base preparation, super heated hydrogen mounting and the cap washing facilities; none of them are known to be positive corrective action. Also, the surface study program in the contract was directed toward an understanding of the conditions causing this failure mechanisms. But, to be effective toward meeting the desired goals, it would have to be accelerated and expanded beyond a study program. Accordingly, the following action has been taken.

Engineering Status. The surface study program was reviewed to place emphasis on those problem areas which have the greatest effect on product reliability. In the surface study program, the primary problem area (see failure analysis section 3.3) is the surface degradation of the collector diode. In contrast to other problems (spur regrowth and emitter wisps) which were not planned at the beginning of the contract, the new emphasis on this problem was done within the framework of the originally proposed surface study program. The considerations for the review of the program were as follows:

1. Where a problem can be identified which related to diode degradation (failure mode 3.2), an engineering assignment will be made to that item. The problem areas are moisture control, metal ion control, and mounting atmosphere control. Since atmosphere improvements were already included in the program plan (mounting furnace 3.1.13), no changes in the plan were made for this item.

2. The empirical studies will be accelerated to allow time for process improvements in terms of the contract termination. The time base for the empirical studies was changed by increasing the effort so that the first series of experiments will be completed and analyzed by the 32nd week of the contract instead of the 52nd week. This allows time for process evaluation and inclusion of the item in the process in cases where additional experiments or equipment design are not necessary (Paragraph 3.4.7). Where additional experiments are necessary, it will be possible to complete the process evaluation by the 52nd week.

3. Attempts to describe the failure phenomena and the supporting functions required for this will be consolidated into a single study group to insure adequate emphasis on the reliability problem. This group's efforts are detailed in pargraphs 3.4.1 through 3.4.5.

Conclusions. Results and conclusions are detailed in Section 3.4. The results are providing clues of means to alleviate the problem.

Program for the Next Quarter. The revised plan of attack will be continued with strong effort oriented toward the particular problem of diode degradation.

3.1.19 Spur Regrowth - J. M. Hall, W. H. Lynch, R. P. Anjard.

General. A secondary contributor to reliability type failures is attributed to "spur" regrowth, particularly in the collector areas. In an effort to meet the reliability goals of the contract, emphasis has been placed on correcting this problem. The problem was not included in the original plans, except for possible incidental influence from the alloy boat and alloy furnace programs (3.1.10 and 3.1.11).

Spurs of germanium emanating from the regrowth area occur during the alloy cooling cycle on the 2N1358 element. This unwanted germanium regrowth condition that occurs predominatly at the junction periphery represents a reliability problem because it may cause a crack which will penetrate into the collector junction and cause transistor failure.

Junction failures due to this cause may be reported as excessive junction leakage current or as high floating potential. A discussion of these two types of failures related to small collector defects that may be caused by small cracks induced by spur regrowth follows.

Units which have failed the floating potential test exhibit collector diode voltage-current "breakup" when traced on a Tektronix curve tracer. This "breakup" is due to oscillation in the curve tracer circuit because of a negative resistance region in the VCBO-ICBO characteristic of the transistor under test. This negative resistance is caused by excessive heating in a small area of the collector diode junction. It is postulated that the collector junction develops a small damaged region due to the spur regrowth condition that conducts the majority of the measured junction leakage current at a very high current density and consequently develops high temperature in the damaged area. The reason that this small damaged region may be reported as a floating potential failure without necessarily exceeding junction leakage current limits is explained by referring to Figure 3-1-A which represents a transistor with a localized collector defect undergoing the floating potential test. Since the small defect has a high spreading resistance due to its small size and since most of the collector leakage current will flow through it, a high floating potential will develop even though the collector leakage current may still be within specification. A simplified equivalent circuit of this measurement is presented in Figure 3-1-B. The floating potential induced by this mechanism may cause operational failures by overcoming the reverse bias voltage normally applied to the emitter in operating circuits to cutoff or hold the transistors at cutoff.

FIGURE 3-1-A

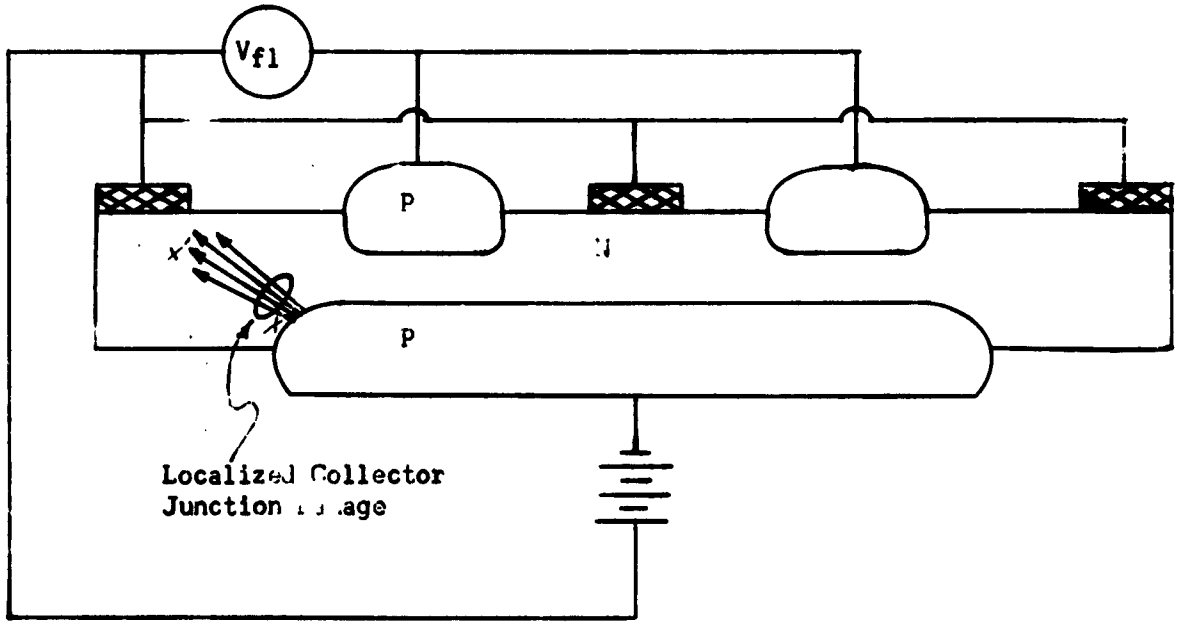
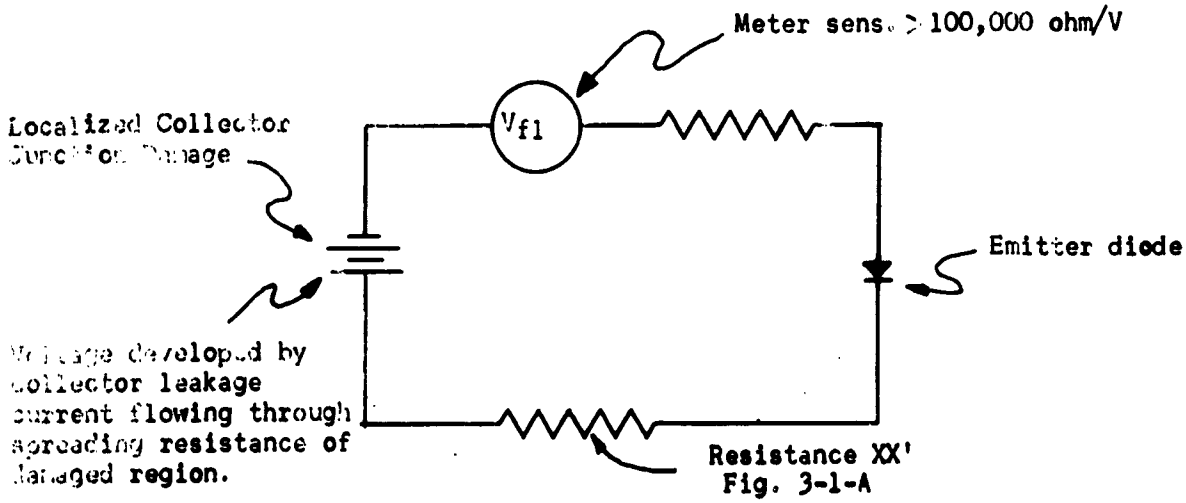


FIGURE 3-1-B



Collector diode failures induced by spurs are simply a manifestation of the same type of damaged collector junction, but over a larger area with an attendant smaller spreading resistance value such that the collector junction leakage current exceeds the limit. Due to the lower value of spreading resistance associated with larger collector faults, the floating potential may not exceed the floating potential limit on the collector diode failures. The larger the collector diode fault, the more likely it will be reported as a collector diode failure, and less likely to be reported as a floating potential failure.

Since collector diode degradation and high floating potential are likely to lead to operational failure, it is highly desirable that the spur regrowth condition be eliminated. A hypothesis on the growth mechanism of spurs and how to go about eliminating them follows.

Engineering Status - W. H. Lynch. A detailed microscopic analysis was made on germanium crystal regrowth from indium solutions with the prime purpose of attempting an explanation of the mechanism peripheral or "spur" regrowth formation in transistors.

Spur regrowth, to some extent, is always present on the 2N1358 type transistors made by the production process. Many attempts have been made in the past to control the cooling rate of standard geometry 2N1358 type transistors in an effort to eliminate spurs. A reduction in the size of individual spurs has been noted when extremely slow cooling rates have been used (the order of 1°C - 2°C/minute). A reduction in spurs is also seen when thinner indium is used in conjunction with higher alloy temperatures. Effectively this causes an increase in the germanium growth rate from solution as indicated by the In - Ge phase diagram.

Thickness of the regrowth region also has an effect on the extent to which spurs may grow. Radio grade type transistors experience near identical temperatures and cooling rates during alloy as the 2N1358 types. Spurs, when they are present in the radio grade units, are very small. The thickness of the regrowth germanium in the 2N1358 type is about 2.4 mils, and in the radio grade it is about 1.2 mils, approximately one-half.

Information from the literature[1,2] indicates that growth rates in the three major crystallographic planes in germanium are not the same. Growth rates from solution under slow cool conditions are approximately five times faster in both the 110 and 100 directions, than in the 111 direction.

The regrown region of transistors was observed in both cross-sectioned views and after indium alloy removal. Of course, in a cross-section, only one increment of each transistor is seen; however, by looking at a large number of individual samples, this limitation is overcome. As it turned out, examples of the hypothesis of spur growth that was developed from these observations can be seen in almost every cross-sectioned transistor.

Figures 3-1-C and 3-1-D are photomicrographs of the type of spur growth in question. Figure 3-1-E is a top view of spurs after the indium alloy has been removed. It is clear that the relatively large cantilever structures of the spurs are supported by very thin areas, and a downward force could fracture the spur. Since the junction is very close to the support area, in most cases, a fracture would cause damage to the critical junction-surface intersection. In Figure 3-1-E, a tendency for spur

[1] Jacques I. Pankove, RCA Review, March, 1954
[2] B. Goldstein, RCA Review, June, 1957.

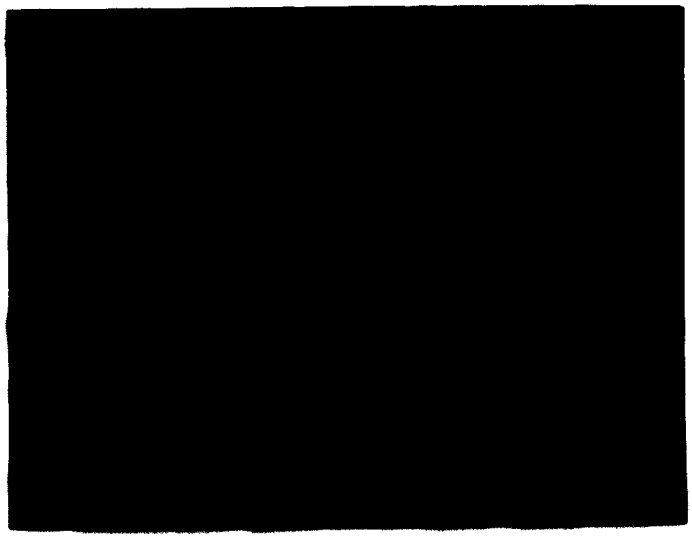


Fig. 3-1-C

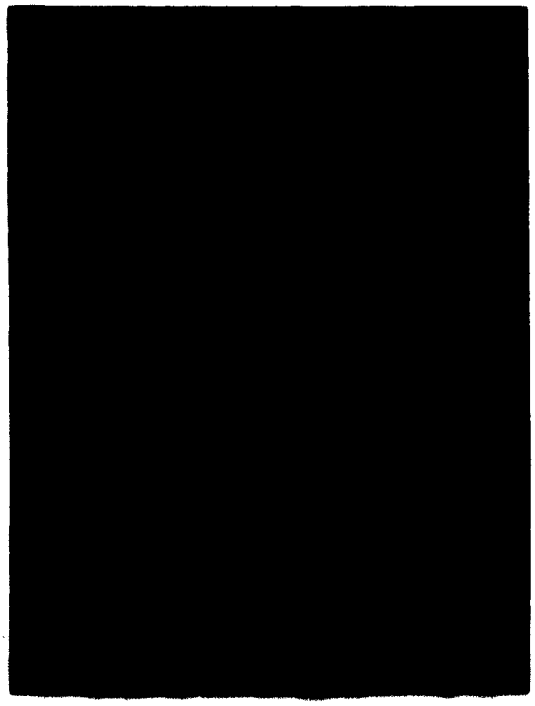


Fig. 3-1-D

Fig. 3-1-E

edges to form 120° angles can be seen. This indicates that the spurs grow in 110 plane directions since there are six 110 planes in the lattice angularly spaced at 120° that are perpendicular to the 111 planes.

The occurrence of spur regrowth is not limited to the outer edge of an alloyed junction, as would be the case if thermal gradients were the determinants of the condition. Figures 3-1-F, 3-1-G, and 3-1-H, are examples of internal spur growth. From these photomicrographs, it can be seen that spurs are associated with irregularities in the terminal solid-liquid interface (junction). Obviously there must be an irregularity in the junction when it comes to the surface around its periphery. Therefore, when growth conditions are suitable for spur formations, they are always present at the periphery. Furthermore, the size of the spurs is proportional to the size of the junction irregularity making the peripheral spurs larger than internal spurs in a given specimen.

A close examination of the regrown area reveals a means of tracking the growth process. After a specimen has been etched to show the junctions, other lines can be seen faintly in the regrowth. These lines are low angle grain boundaries, and they delineate the point where two separately nucleated areas grow together. On the boundary line, the lattice from one area is slightly mismatched with its neighbor. Figures 3-1-I and 3-1-J are examples of low angle grain boundaries in the regrowth. Figures 3-1-K and 3-1-L show that the boundary lines terminate at the corners of overlapping plates. These two photographs, of course, are of the terminal solidification case, but it must be assumed that a similar condition could exist during early stages of crystal regrowth. The origination of boundary lines, in most cases, can be traced to junction irregularities, and are usually tangent to the high point in the junction irregularity.

Fig. 3-1-F

Fig. 3-1-G

Fig. 3-1-H

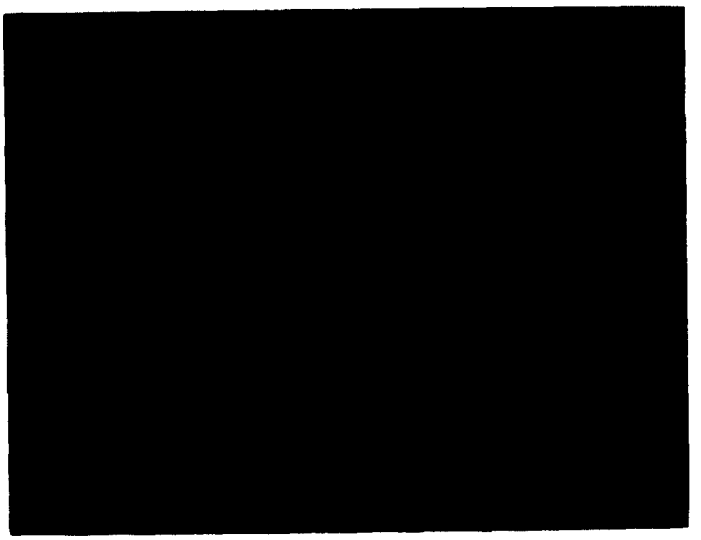


Fig. 3-1-I

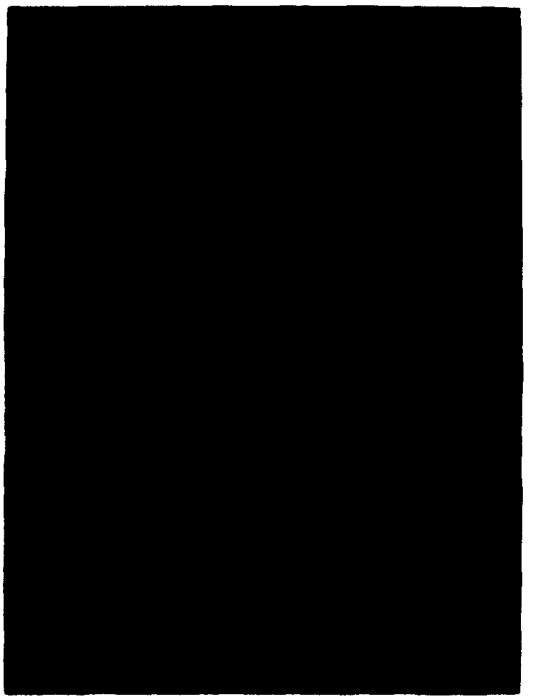


Fig. 3-1-J

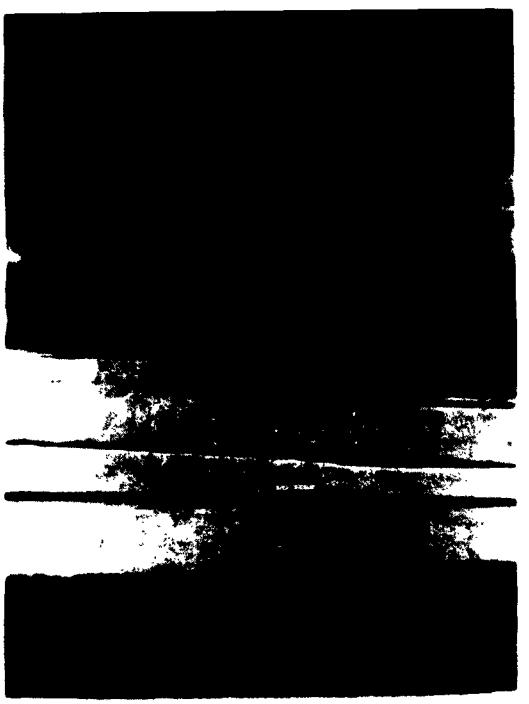


Fig. 3-1-K

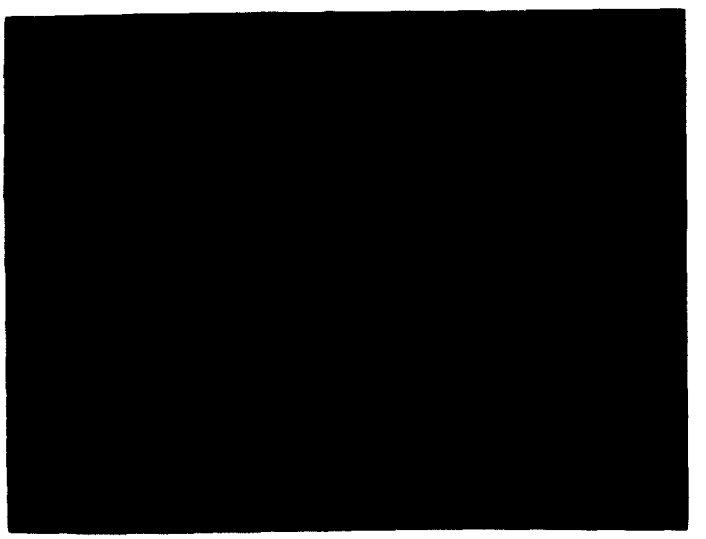


Fig. 3-1-L

Occurring simultaneously with spur crystal formation are large voids in the germanium regrowth. Figures 3-1-M, 3-1-N, and 3-1-O, are examples of voids in germanium regrowth. It is interesting to note that in visualizing the crystal as it regrows from the melt that the spur does not develop fully until a growth void is initiated. In other words, it is the mechanism that causes the void that is the real problem in controlling spur regrowth.

Figure 3-1-P is a sketch illustrating the formation of a growth void and subsequent spur development. This is an idealized case with one junction irregularity, and it shows the regrown crystal at various stages of growth. An attempt is made to show the function of the two mechanisms that according to the hypothesis lead to spur formation; i. e., a higher growth rate in 110 direction and a lower germanium concentration in the liquid near the inside corner. As shown in Figure 3-1-P, the upper corner of the irregularity grows faster than the lower corner until either the spur blocks the lower corner off from further germanium migration or the lower corner develops a 111 plane, thereby slowing its growth. At this point, no further growth takes place at the lower corner and a void develops. Once the void is initiated, the spur is free to exaggerate in size with further germanium solidification.

Under any specified conditions of temperature and cooling rate, some regrowth thickness is necessary before voids and subsequent spur development can take place. Therefore, when overall regrowth thickness is reduced, such as in the radio grade type unit, spur development is minimized.

The effects of the two mechanisms involved in spur growth; i. e., faster 110 plane growth and lower germanium

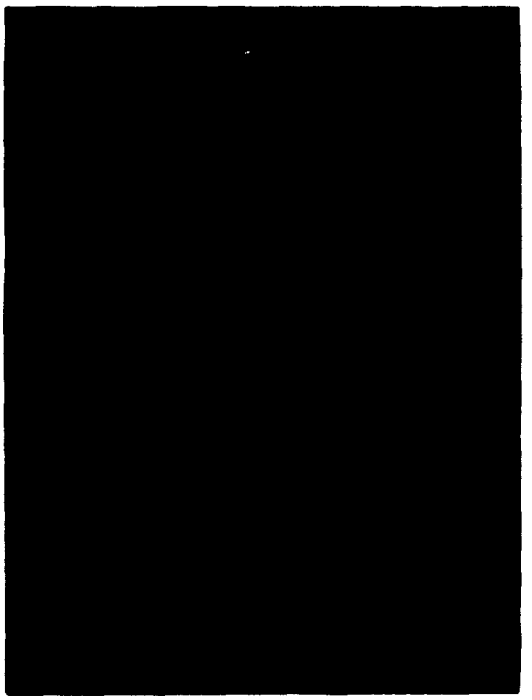


Fig. 3-1-M

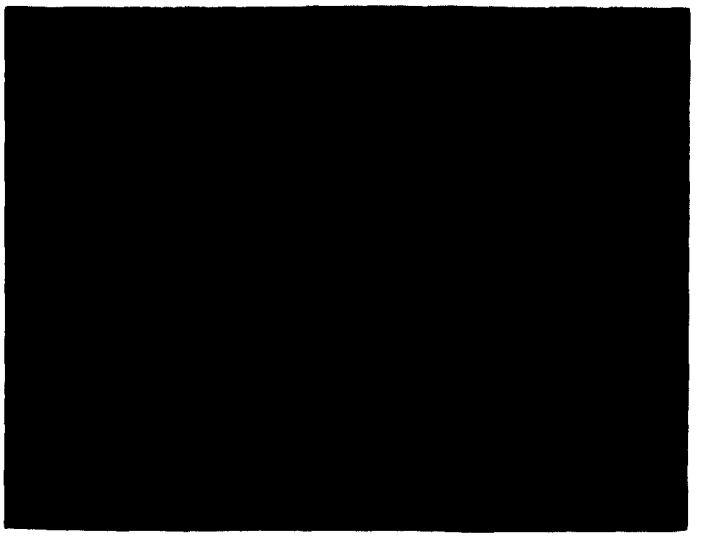


Fig. 3-1-N

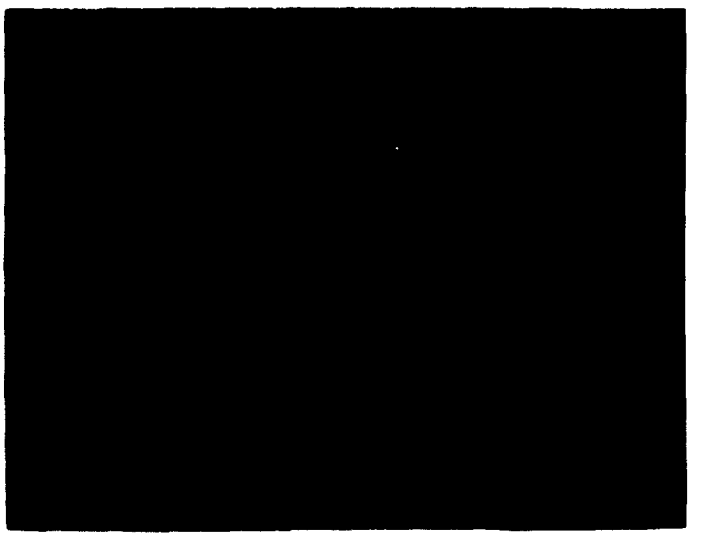


Fig. 3-1-O

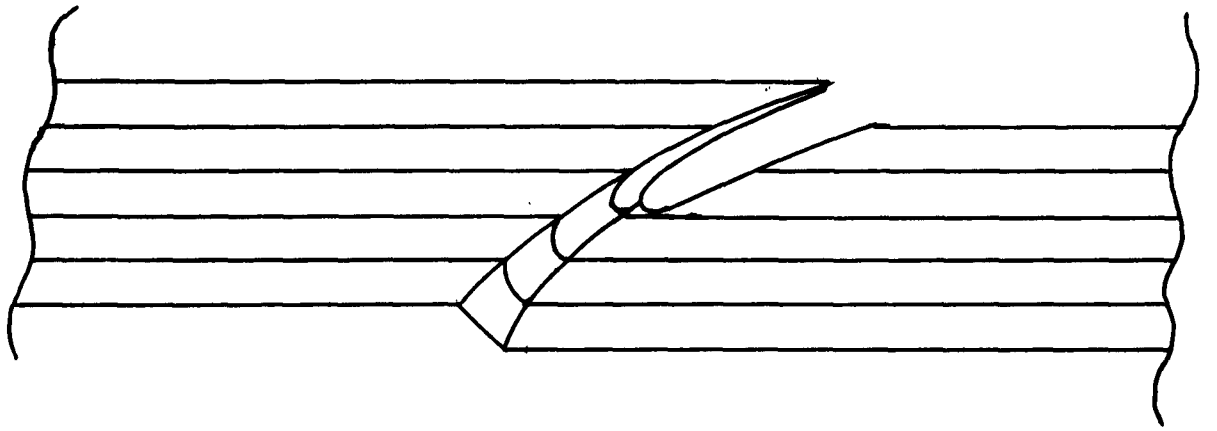


Fig. 3-1-P

concentrations at the inside corner, are inversely proportional to each other as the crystal growth rate is varied. At low rates of crystal growth from solution, the 110 plane growth would approach a maximum differential when compared to the 111 growth rate. The literatures [1,2] indicates that the differential can be as high as five times as fast in the 110 directions. But at the same, slow growth rates would allow for germanium diffusion in the liquid to the inside corner and thereby tend to enhance crystal growth at this point. The effect of the diffusion mechanisms must predominate in the slow growth condition because spur growth is reduced. Conversely, a fast growth condition would tend to reduce the differential in a plane direction growth and delay void formations. This is verified by high temperature alloyed transistors which do undergo a more rapid growth rate, as indicated by the indium-germanium phase diagram. High temperature alloyed units do exhibit a minimized spur structure.

Conclusions. It is concluded that spur formation is a natural phenomenon determined by the rate of crystal growth from solution and the difference in growth rate of the various crystallographic planes involved in the germanium lattice. It is further concluded that there is a tendency for spur formation at any area of regrowth near a deviation from planarity of the terminal solid-liquid interface. Elimination of the spurs probably lies in the direction of a change in the rate of crystal growth from solution.

As a result of the analysis of the problem, elements were alloyed using thinner indium in place of the standard thickness of

[1] Jacques I. Pankove, RCA Review, March, 1954
[2] B. Goldstein, RCA Review, June, 1957

indium for the collector and emitter. The standard wafer thickness was used so a higher alloying temperature was required to produce the normal base width. Alloy regrowth conditions were established by these changes, such that the alloyed elements did not exhibit spur regrowth. When these elements were mounted and etched, the emitter wisps were reduced by 47%, which indicates that this change may simultaneously solve two problems.

Program for the Next Quarter. An experiment will start in the near future using these techniques on 1000, 2N1358 alloyed elements in order to fully evaluate the effects on reliability and yield.

3.1.20 Emitter Wisps - R. P. Anjard.

General. Another secondary contributor to reliability type failures (observed decellerated rate of .000206 failures per 1000 hours at use conditions of 10V-1A-41°C) is attributed to very small filaments of indium or indium-germanium that protrude from the emitter on some of the transistors. Again, effort on this particular problem was not included in the original program plan, but is important to solve for reliability improvement. These protrusions, under certain conditions, can cause a high resistance ohmic condition. There is, also, some evidence that show wisps are responsible for some of the observed emitter diode degradation.

Engineering Status. The base line of the problem has been established and the current value for the 2N1358 basic unit has

been normalized to a value of 1.0. The following facts have been established and referenced to the normalized value of 1.

(a) .57 of present radio grade (when etched as 2N1358's) have wisps. Note that the indium composition is the same for both. The main differences being that the radio grade has approximately one-half of the indium, considerably dewets, and exhibits very little, if any, spur regrowth.

(b) .07 of the radio grade have wisps

(c) .07 of 2N1358 (when etched as radio grade) have wisps.

Further defining these wisps, the origins for the wisps on the standard 2N1358 are as follows:

Description	% of all Wisps	% of class which can touch: Germanium	Base Contact
Solder from indium mass at dewet area	19	15	0
Solder continuum[1] on periphery at dewet area	32	18	6
Interrupted solder continuum[2] on periphery at dewet area	32	12	0
Solder continuum at non-dewet area	4	0	0
Non-dewet area	13	43	0

[1] A solder continuum is defined as a thin segment of solder which is connected to the main indium mass. These may be found on the regrowth or on the outer periphery of the regrowth, either at a dewet or non-dewet area.

[2] An interrupted continuum is a thin solder segment as above, but has been disconnected from the source.

Total wisps from dewet area	73.0
Total wisps from non-dewet area	27.0

In comparison, the 2N1358 when etched the same as the radio grade, which uses a lighter etch, has a distribution of wisp origins as follows:

Description	% of all Wisps	% of class which can touch: Germanium	Base Contact
Interrupted continuum - dewet area	90	0	0
Solder continuum - dewet area	10	0	33

The actual distribution of the number of wisps per emitter is also presented for units with wisps:

No. of Wisps/unit	Distribution (%) of units with # of wisps/unit	
	2N1358	2N1358 (etched as radio grade)
1	72	87
2	19	13
3	5	0
4	4	0

Correlation of Wisps to Other Factors: Wisps have been observed on other transistors manufactured by Delco Radio and other manfacturers.

Very few wisps have been detected on the collector diode. This is because the degree of etching is much less and the degree of dewetting on the collector is, also, much less. Basic units, which have no detectable dewetting on the emitter, have wisps before etching but the frequency and size of wisps are reduced.

Probable Causes of Emitter Wisps: From an examination of the emitter surface and cross-sections, it has been found that the majority of wisps occur either from (a) indium left on the periphery when the emitter indium dewets or/and (b) indium restricted by spur regrowth in combination with (c) undercutting by the etch. Figure 3-1-Q shows an element cross-section, partial dewetting, and a wisp caused by undercutting. In Figure 3-1-R, the effect of this undercutting is dramatically illustrated.

A segreation of the solder has been observed at the periphery of the dewet indium mass. A large portion of the generated wisps originate from continuums which remain on the outer side of the spur regrowth. Attached photographs show this segregation which has been found to be a high germanium content alloy by X-ray diffraction analysis.

Photographs 3-1-S and 3-1-T show this segregated phase. The ability of the solder to form filaments and potential wisps is exhibited in Photographs 3-1-T and 3-1-U. The actual occurrence of a wisp showing its origin from the dewet area is illustrated in Photographs 3-1-V and 3-1-W. A wisp that nearly touches the center base contact is shown in Figure 3-1-X. Although these pictures show etched 2N1358 basic unit emitters,

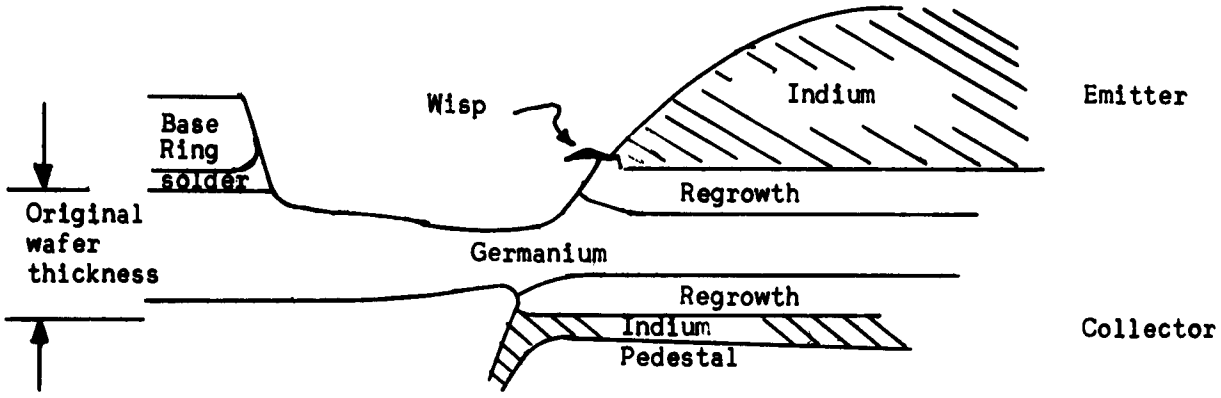


Fig. 3-1-Q

Wisp generated at dewet area Note the depth of etching.

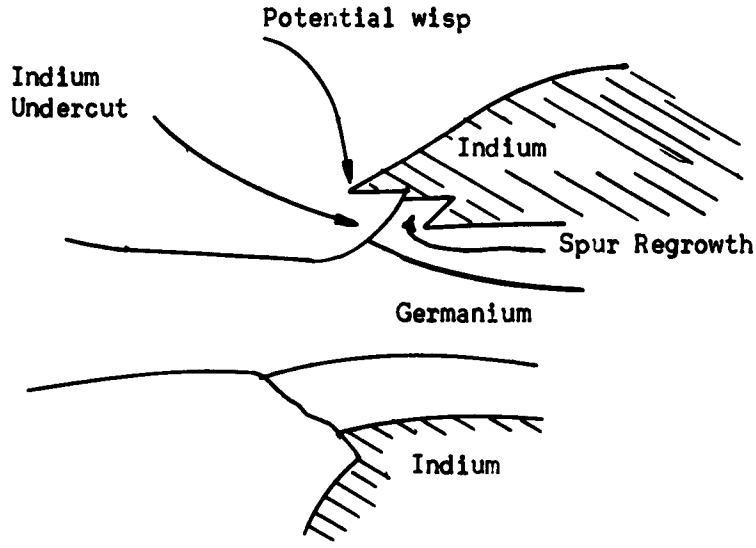


Fig. 3-1-R

This cross-section of an element shows how undercutting the emitter can cause wisps.

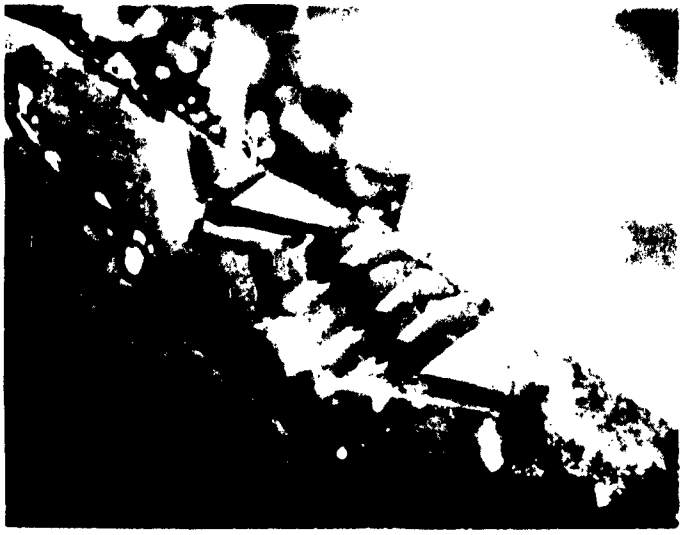


Fig. 3-1-S

Enlarged view of segregated phase on the germanium regrowth section.

Fig. 3-1-T

Segregated phase on the germanium regrowth exhibiting small protrusions. Also note the presence of solder on the periphery of the regrowth.

Fig. 3-1-U

The ability of the solder to form filaments is also demonstrated in this enlargement of a dewet area.

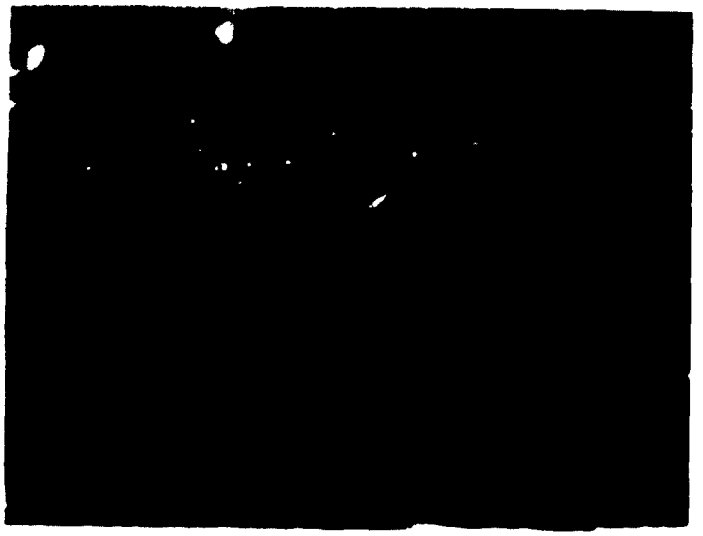


Fig. 3-1-V

A wisp on the inner periphery of the emitter ring is shown. This is an example of a "solder continuum".

Fig. 3-1-W

A wisp on the outer periphery originated from a dewet area.

Fig. 3-1-X

A wisp is in close proximity to the center base contact. This wisp originated from a non-dewet area.

the collector diode on rare occasion has exhibited a wisp (Photographs 3-1-AA and 3-1-BB). An unetched transistor element is shown in Photograph 3-1-CC to indicate the presence of the periphery solder at that stage.

Experimental Approach and Results:

Etching:

1. An experiment in which a lighter emitter etch was used is being evaluated to compare resulting electrical parameters and wisp generation with the standard product. Data on this experiment is not completed.

2. Following the production etching, units were subjected to 1:1 HCL in H_2O at room temperature. After 5 minutes immersion, approximately 60% of the wisps were partially removed, within 1 minute new protrusions were generated at undercut sections by additional etching.

3. Electrolytic etching of the emitter only in 1% HCL for 30 seconds with 0.5 amp removed all the wisps, but the germanium surface was back plated with a metallic film. A typical diode characteristic after this treatment was approximately 20V at ICBO = 4ma, which is not acceptable.

Alloying.

1. A comparison of the 2N1358 and the radio grade for

Fig. 3-1-AA

Low magnification view of an element to show the presence of a wisp.

Fig. 3-1-BB

This is an enlargement of photograph 3-1-AA.

Fig. 3-1-CC

A "solder centinuum" on the periphery of the re-growth area prior to etching is shown at approximately 50X. Note the degree of dewetting.

wisps and spur regrowth lead to the evaluation of the 2N1358 alloyed with thinner indium at a higher temperature. Although the units dewet considerably upon mounting as do the radio grade units, the quantity of wisps were reduced to 47% of the present value. A sample of these "modified" elements were processed through dissipation and thermal stress without failure. One thousand additional elements are being processed for complete evaluation.

2. Very small additions of aluminum were made to the standard alloy. Although the alloy used was not a homogeneous mixture, as evidenced by the localized wetting and non-wetting during alloy, these elements when etched did not exhibit wisps. Indium alloy with a small percentage of aluminum, which is homogeneous, has been received and punched. Extensive alloy experiments have been initiated. Acceptable elements will be processed, etched, electrically evaluated, and then examined for wisps. Other samples have been ordered from suppliers for additional studies.

Elimination of Dewetting. Since the amount of wisp on the 2N-1358 was seemingly correlated to the amount of emitter indium dewetting, numerous experiments were run to eliminate dewetting.

1. The following types of plating on the emitter convector were not satisfactory for the elimination of indium dewetting during mounting:

   (a) 0.0001" tin
   (b) 0.0005" nickel

(c) 0.0001" nickel
(d) 0.0001" nickel, overplated with 0.0001" cadmium
(e) 0.0001" 60% tin-40% nickel

The tin-nickel alloy (e) did not actually dewet, but due to the pressure exerted by the emitter connector with non-wetting of the indium to the plated surface, shorting resulted, usually filling in the entire ring. Various attempts to modify the emitter foot resulted in almost complete dewetting or 100% shorting.

2. Coating the emitter connector with various solders of the tin-indium series were unsatisfactory due to excessive dewetting.

3. The emitter foot was closed and the width was increased to closely match the O.D. and I.D. of the emitter indium. Shorting generally resulted during mounting, even when parts were silver plated.

4. The closure of the emitter foot ring did not reduce dewetting; shorting occurred during processing.

5. Reduction of the emitter connector foot generally caused excessive dewetting.

6. Modification of the emitter alloy with aluminum was discussed previously.

7. To obtain a smaller sink for indium, the width of the emitter connector was decreased 50% and 67% without significantly reducing the dewetting.

8. Elements and emitter connectors were oxidized at 120°C for 16 hours. All three combinations were unsatisfactory.

9. Transistors which did not exhibit dewetting did exhibit wisps after etching, as mentioned. Attempts are being made to obtain sufficient units so that the actual percentage, size, etc., can be determined.

Spur Regrowth Elimination (as it pertains to wisps):

1. The "modified" elements using thinner indium (4.2.1) do not exhibit spur regrowth. Thus, there is little restriction to the withdrawal of indium from the periphery as shown in Photograph 3-1-DD.

Removal of Wisps on Etched Units Prior to Capping: Some thought was given to the elimination of the wisp after it has been generated prior to capping the unit. However, the main emphasis was, and still is, to prevent the formation of wisps. Results of experiments in this area are as follows:

1. Re-etching was described. The addition of an oxidizing agent, H_2O_2 to the HCL removed the nickel from the base.

2. Impingement on the emitter by a high velocity air stream for 15 seconds removes all the large wisps, but does not completely eliminate small protrusions. This technique is unsatisfactory from a reliability

Fig. 3-1-DD

Although considerable dewetting is present, very little solder was restricted on the periphery as the spur regrowth was significantly reduced.

standpoint due to the potential encapsulation of these loose filaments.

3. Attempts to remelt the indium by the impingement of a hot air jet were conducted to cause the wisp to be melted, and thereby cause it to be withdrawn to the indium mass, were likewise unsuccessful. In general, this hot force of air melted surrounding solders causing shorts, loose center contacts, etc.

Conclusions.

1. The main cause of wisps is the undercutting of the indium by the etch. Reduction of spur regrowth and more effective dewetting reduces wisp generation. It was originally hypothesized that the main cause for wisp generation was dewetting. Devices with aluminum in the emitter alloy do not dewet or have wisps. However, the heavy oxide caused withdrawal of solder to be internal rather than at the periphery. If dewetting could be eliminated on the standard 2N1358, the limited available data and the present understanding suggest that wisps will still be generated. Chemical or air removal of the wisps is not satisfactory on the basis of yield and reliability.

Program for the Next Quarter. As indicated, 1000 elements are to be alloyed using thinner indium and will be completely evaluated to insure that other reliability factors are not adversely affected. Also, extensive experiments using small percentages

of aluminum in the alloy will be conducted to determine the effect on wisp and spur regrowth generation, in addition to the effects on electrical relationships, such as the emitter efficiency. But this is not a short range solution. Investigations of reduced emitter etching will also be continued. Attempts will be made to more adequately evaluate wisp generation on units with none or little solder dewetting.

3.2 RELIABILITY TEST PROGRAM.

3.2.1 Failure Rate Goals - L. V. Ingle.

General and Engineering Status. Milestone I has completed 1000 hours at the 135°C storage and 40V-.5 amp-90°C D.C. operating conditions. Of 289 transistors placed at 135°C, 14 failed to the limits defined in the First Quarterly Report. The failure rate at the 90% confidence level was 6.99% per 1000 hours. This figure is below the stated level at the beginning of the contract (7.88% per 1000 hours), but above the goal for Milestone Test I (4.5% per 1000 hours). All of the failures resulted from high diode leakage current which appears to be the major deterrent to successfully reaching the goals as proposed. The individual readings on the failed units are given in Figure 3-2-A.

The parameter distribution for IC at VC = 80V, IE at VE = 40V, and IB_2 at IC = 5A, VC = 2V, are shown in Figures 3-2-B through 3-2-F. Due to a since corrected error in communications, the initial values of VCBO at IC = 4ma, and VEBO at IC = 4ma, were substituted for IC and IE. It is apparent that the distributions are similar due partly to the test set zener diode truncation at 147 volts. The mean shift between 335 and 1000 hours for IC was .60ma, while the standard deviation increased from .770 to 2.537 (all statistics referenced are with failures removed). The bulk of the mean shift occurred between 666 and 1000 hours - as did the failures. Certainly, this shift is indicative of the major failure mode - diode degradation. IEBO mean shift was only .03ma, while the standard deviation increased just slightly (.062). IB_2 exhibited the units' characteristics movement on accelerated storage.

FIGURE 3.2.A
STORAGE - 175°C
MILESTONE I - FAILED UNITS

UNIT NO.	0 HRS. VCBO ICBO= 4 ma	0 HRS. VEBO IEBO= 4 ma	0 HRS. IB_2 IC=5A VCE=2V	333 HRS ICBO VCBO= 80V	333 HRS IEBO VEBO 40V	333 HRS IB_2 IC=5A VCE=2V	666 HRS. ICBO VCBO= 80V	666 HRS. IEBO VEBO= 40V	666 HRS. IB_2 IC=5A VCE=2V	1000 HRS ICBO VCBO= 80V	1000 HRS IEBO VEBO= 40V	1000 HRS IB_2 IC=5A VCE=2A
02107	147	111	135	1.6	1.8	184	25 +	16.0	200	25+	25+	180
02116	146	87	150	0.5	2.6	176	0.6	2.6	184	16.2	2.8	152
02120	142	146	147	4.3	0.3	180	25 +	20.8	192	25+	25+	176
02136	147	128	127	5.8	1.5	168	20 +	1.8	176	25+	25+	168
02195	131	133	120	0.6	0.4	168	0.6	0.4	184	25+	25+	168
02228	145	137	175	4.2	1.4	200	9.0	0.7	208	17.5	0.2	184
02230	135	84	169	1.8	3.0	200	2.7	1.4	208	25+	3.4	184
02248	145	122	165	0.3	0.3	208	1.2	0.4	212	18.5	0.3	160
02314	141	145	175	0.6	0.3	216	1.8	0.4	224	22	0.3	208
02324	145	129	134	0.4	0.4	160	4.4	0.4	164	25+	0.4	148
02349	146	142	174	0.4	0.3	200	2.2	0.4	204	23	0.4	192
02389	145	102	139	0.4	4.0	172	1.9	2.3	184	25+	15.4	168
02409	145	124	175	0.4	0.6	200	0.4	0.5	200	19	0.4	192
02410	144	145	137	1.6	0.5	184	3.4	2.2	208	25+	25+	192

FIGURE 3.2.B
VCBO INITIAL DISTRIBUTION
135°C STORAGE TEST
MILESTONE I

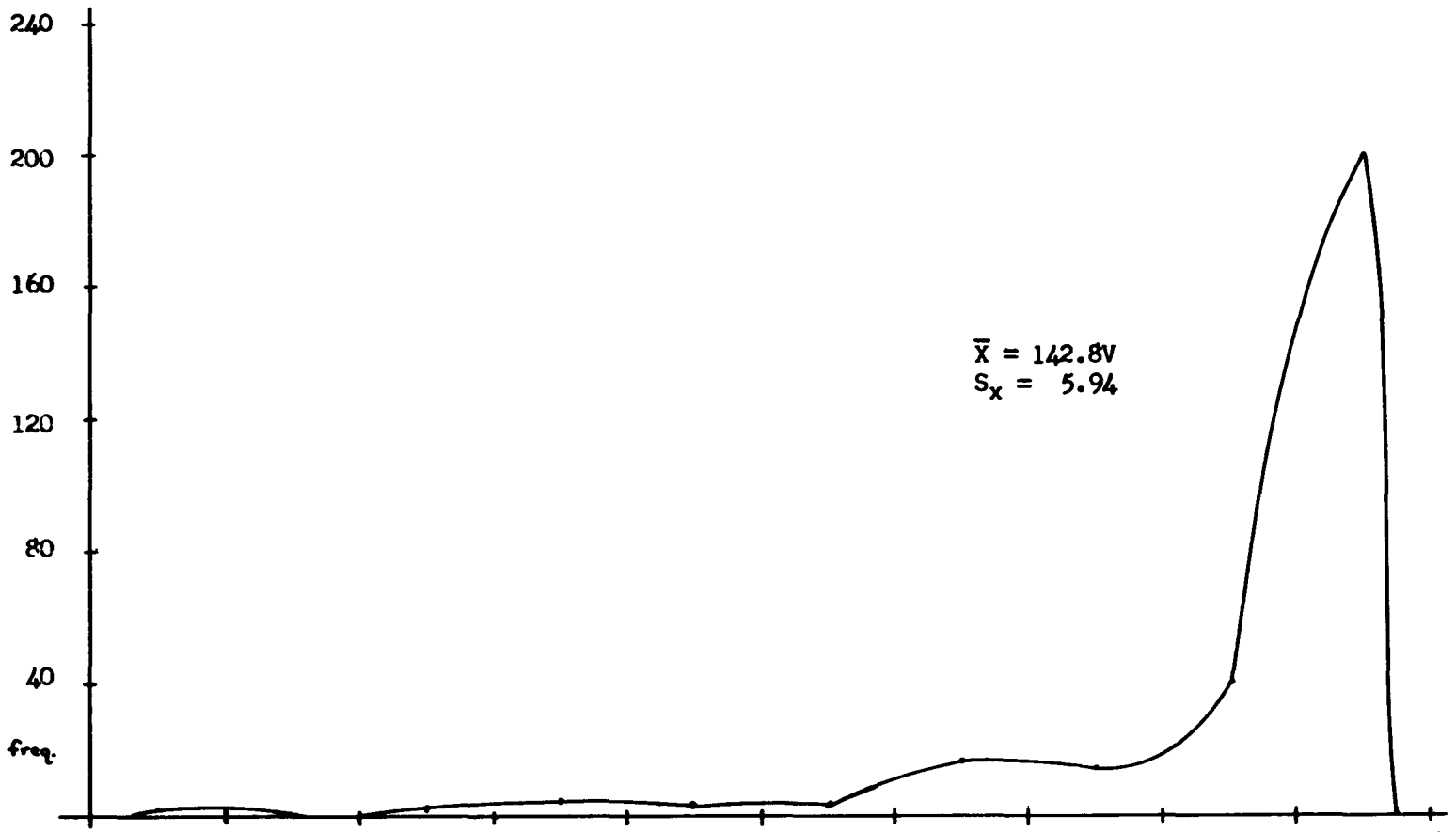
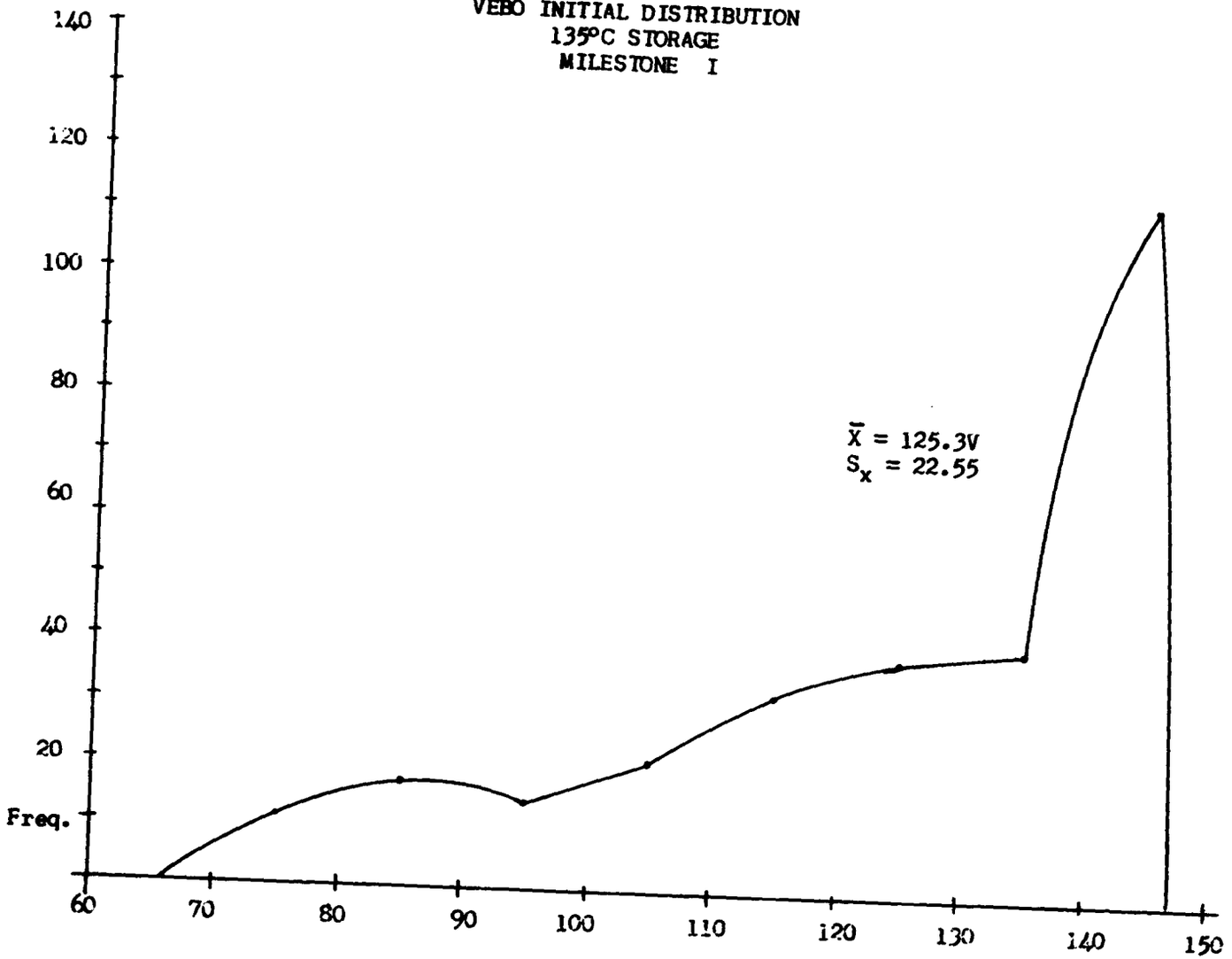


FIGURE 3.2.C
VEBO INITIAL DISTRIBUTION
135°C STORAGE
MILESTONE I



VOLTAGE INTERVAL = 10V
INITIAL DISTRIBUTION

FIGURE 3.2.D
ICBO ON 135°C STORAGE
MILESTONE I

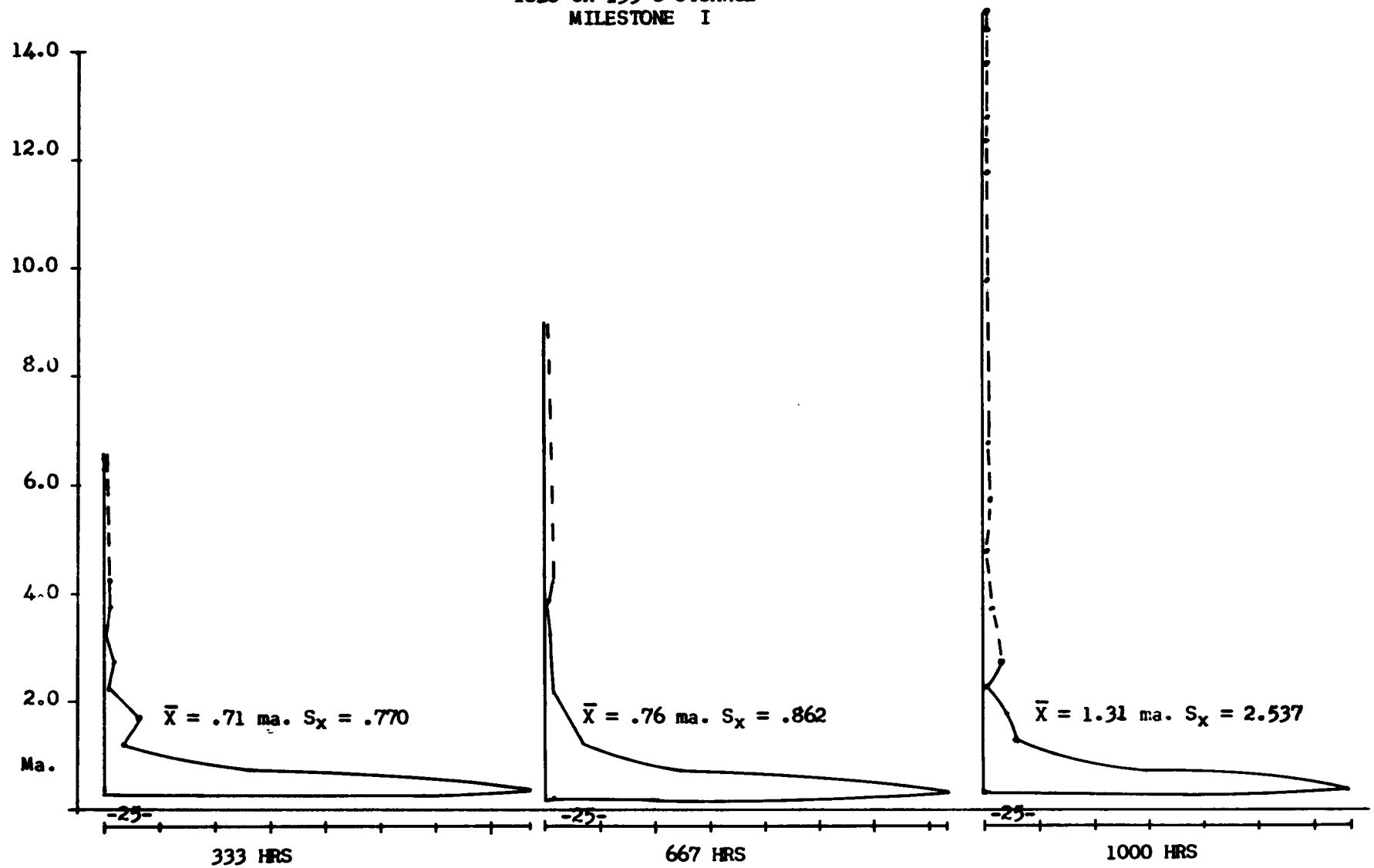


FIGURE 3.2.E
IEBO ON 135°C STORAGE
MILESTONE I

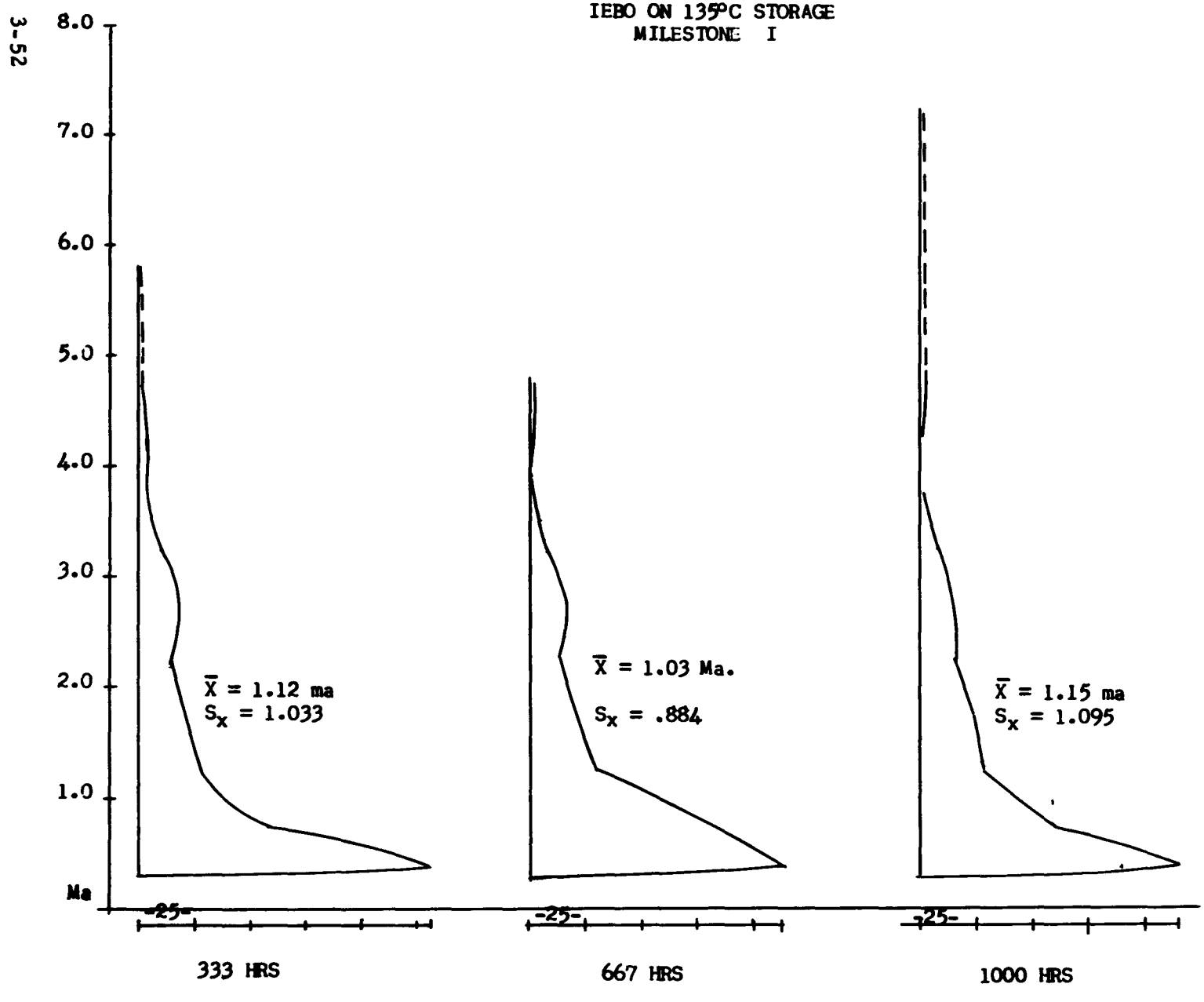
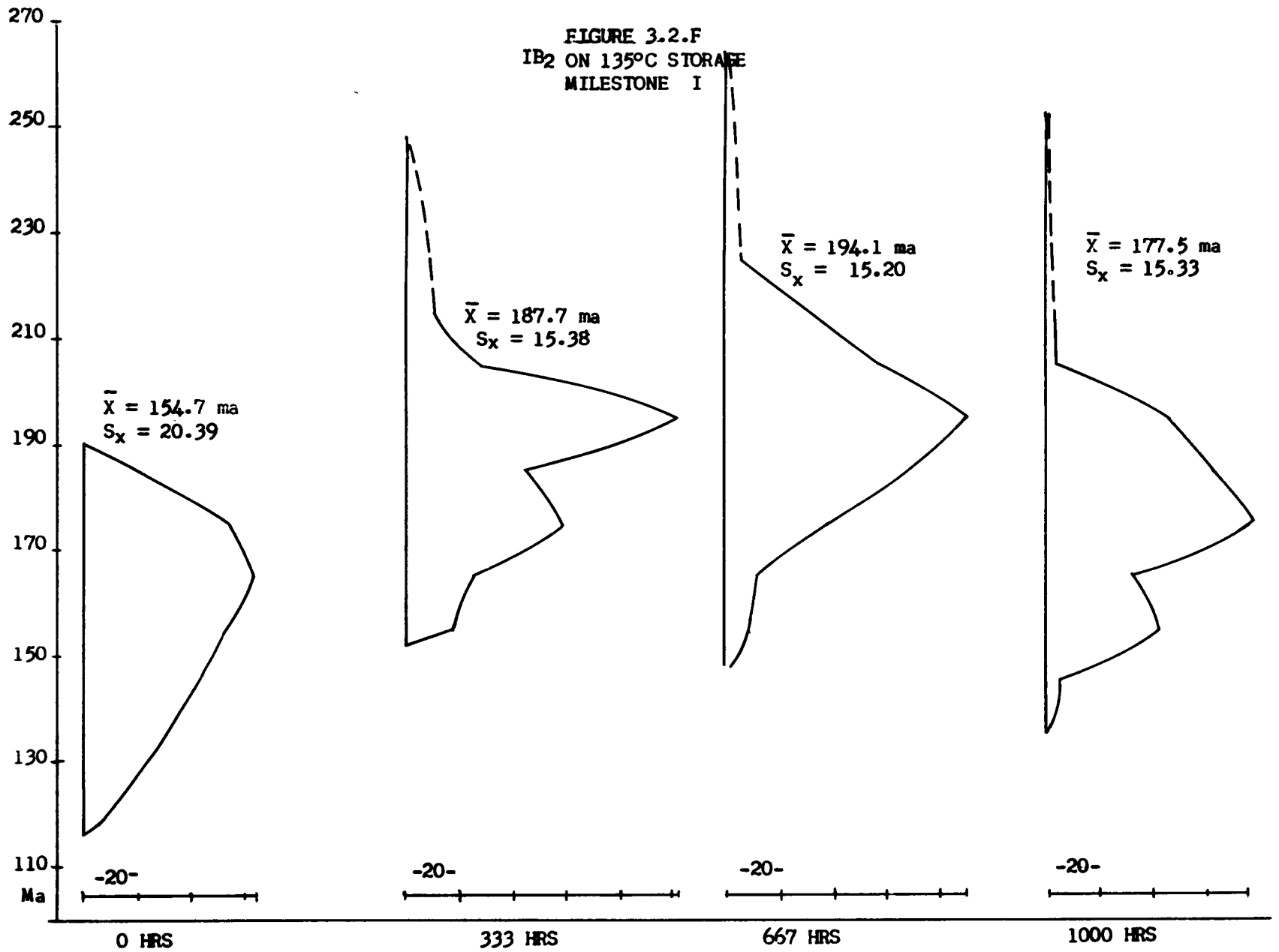


FIGURE 3.2.F
IB_2 ON 135°C STORAGE
MILESTONE I



The mean shifted +36.4ma between initial and 666 hours, and then dropped 16.6ma at 1000 hours. Also, as observed previously, the distribution tightened between initial and 333 hours (S_x = 20.39 to S_x = 15.38) and remained tightened throughout the test.

The transfer and relocation of the D.C. testing chamber induced equipment problems during the early testing hours. More specifically, there were 13 units of the 235 units on test that would not hold a fuse after 24 hours. Five of these devices tested "good" after being dismounted at the 1000 hour test point; and, since the D.C. circuit was open at the fuse, were not on a D.C. test at all. These five units were subtracted from the sample of 235. The failure distribution took the pattern: 8 initial, 2 at 96 hours, 1 at 120 hours, and 1 between 666 and 1000 hours. The resultant failure rate was 7.93% per 1000 hours at 90% confidence. This, again, is below the "present" rate of 8.76% per 1000 hours, but above the goal level of 5.5% per 1000 hours. The eight initial failures are subject for conjecture, as loose base leads and solder shorts (terminal to tray) were found at the completion of testing. Every attempt is being made to remove these elements of doubt before Milestone II testing begins. The failed unit parameters are shown in Figure 3-2-G. All the devices failed due to a form of punch-through producing mechanism.

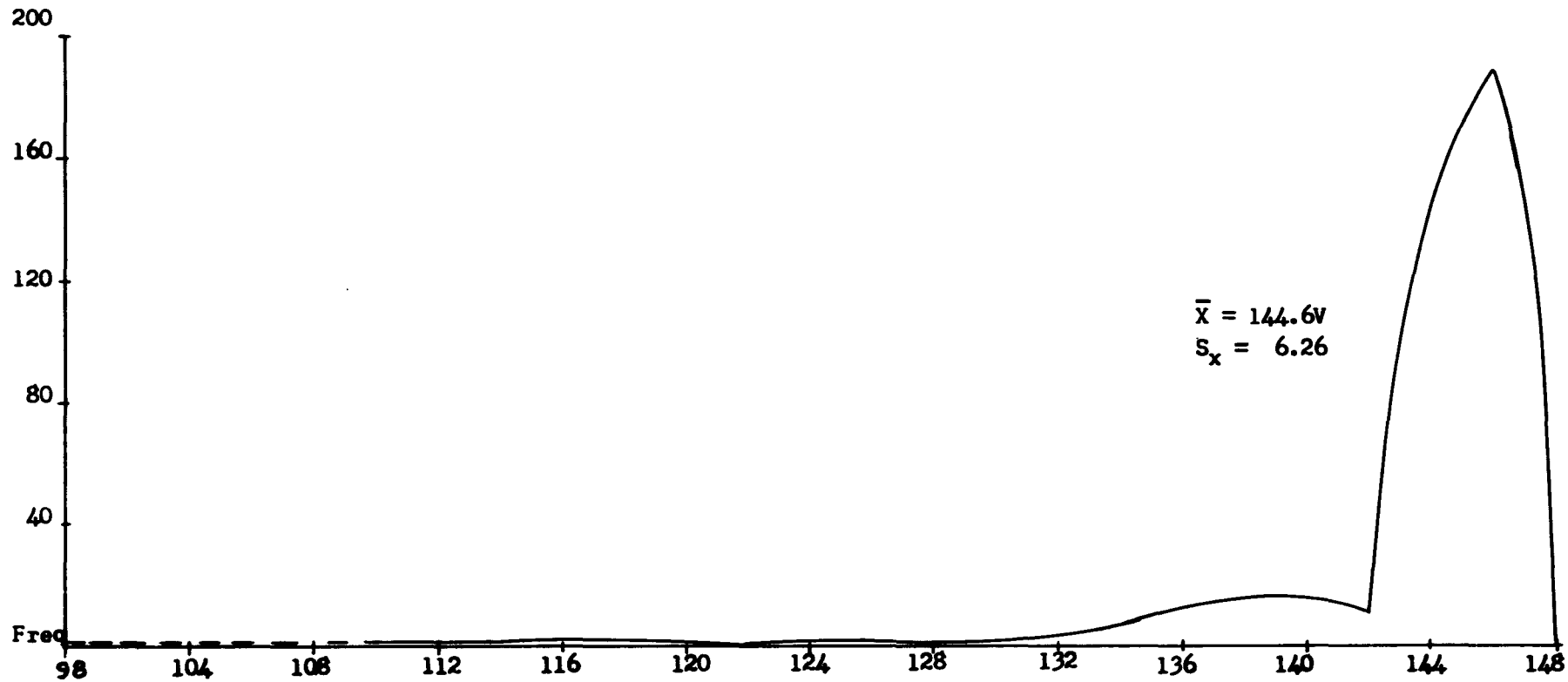
The distributions are shown in Figures 3-2-H through 3-2-L. The initial voltage distributions look much like storage, as expected. The collector current (IC) was much more stable than storage with a mean shift of only .16ma. One unit with IC>8ma at 1000 hours contributed to the standard deviation change from .402 at 333 to 1.007 at 1000 hours. Thus, it appears

FIGURE 3.2.G
20 WATT DC OPERATING LIFE AT 90°C

UNIT NO.	0 HRS VCBO ICBO= 4 ma	0 HRS VEBO IEBO= 4 ma	0 HRS IB_2 IC=5A VCE=2V	333 HRS ICBO VCBO= 80V	333 HRS IEBO VEBO 40V	333 HRS IB_2 IC=5A VCE=2V	666 HRS ICBO VCBO= 80V	666 HRS IEBO VEBO= 40V	666 HRS IB_2 IC=5A VCE=2V	1000 HRS ICBO VCBO= 80V	1000 HRS IEBO VEBO= 40V	1000 HRS IB_2 IC=5A VCE=2A
01816	110	132	158	No Reading -- Open or Short								
01850	144	101	168	No Reading								
01853	147	114	151	No Reading								
01871	146	127	159	No Reading								
01918	144	86	167	No Reading								
01920	147	147	146	No Reading								
01925	147	75	159	NR	3.5	152	NR					
01941	147	83	172	NR								
01984	139	71	180	0.7	3.6	184	0.7	3.6	184	NR		
02034	142	138	139	NR								
02037	129	129	167	NR								
02047	147	147	189	NR								

NR= No Reading

FIGURE 3.2.H
VCBO INITIAL DISTRIBUTION
DC OPERATING TEST
MILESTONE I



VOLTAGE INTERVAL - 10V
INITIAL DISTRIBUTION

FIGURE 3.2.I
VEBO INITIAL DISTRIBUTION
DC OPERATING TEST
MILESTONE I

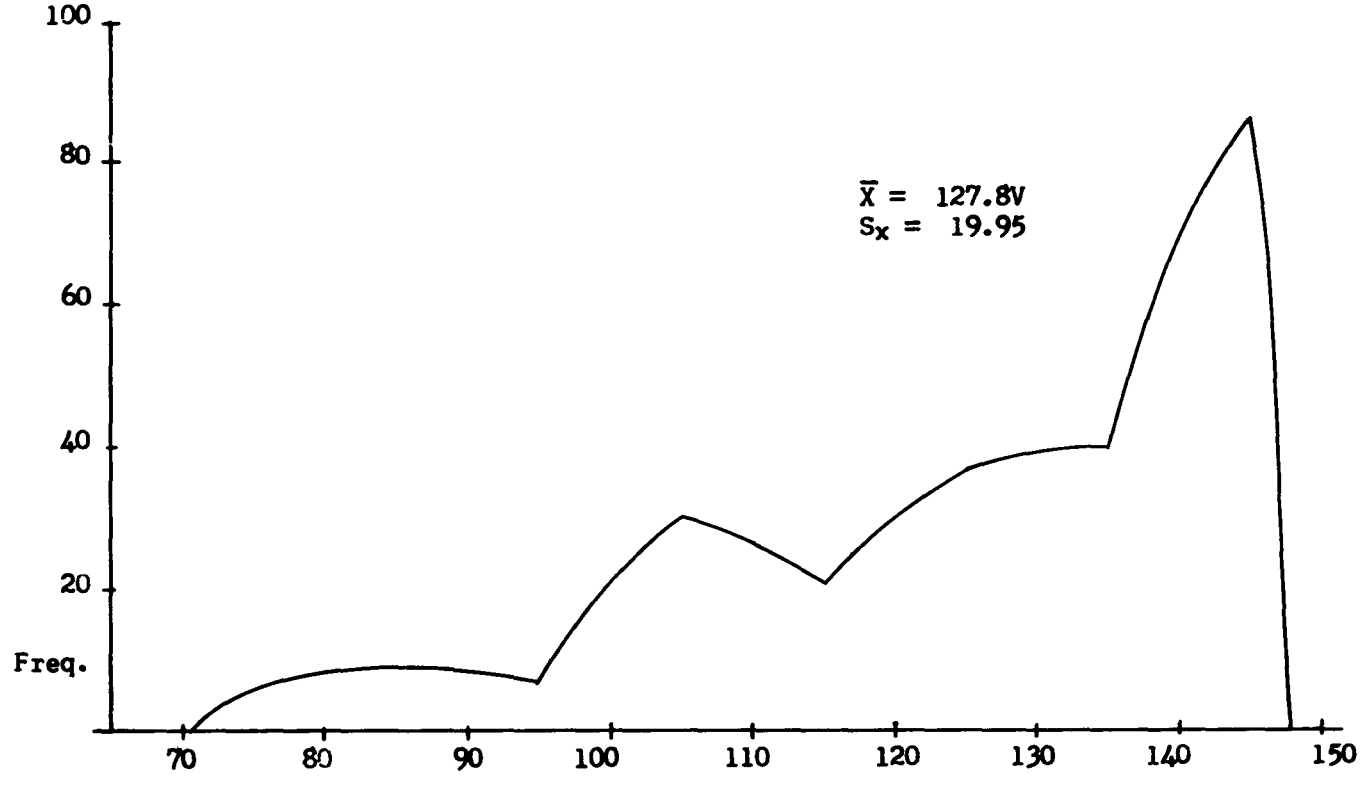


FIGURE 3.2.J
ICBO ON DC OPERATING
MILESTONE I

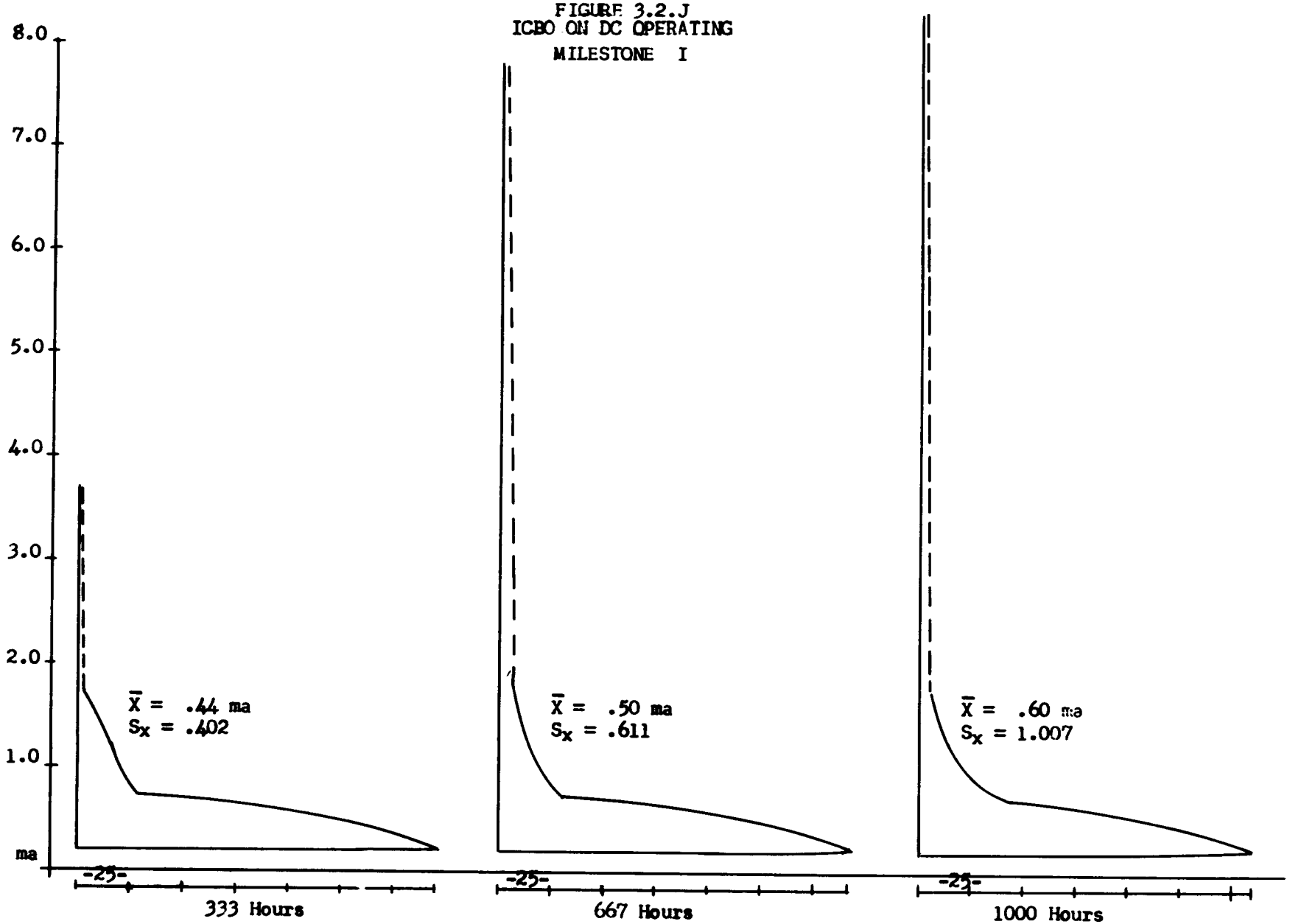


FIGURE 3.2.K
IEBO ON DC OPERATING TEST
MILESTONE I

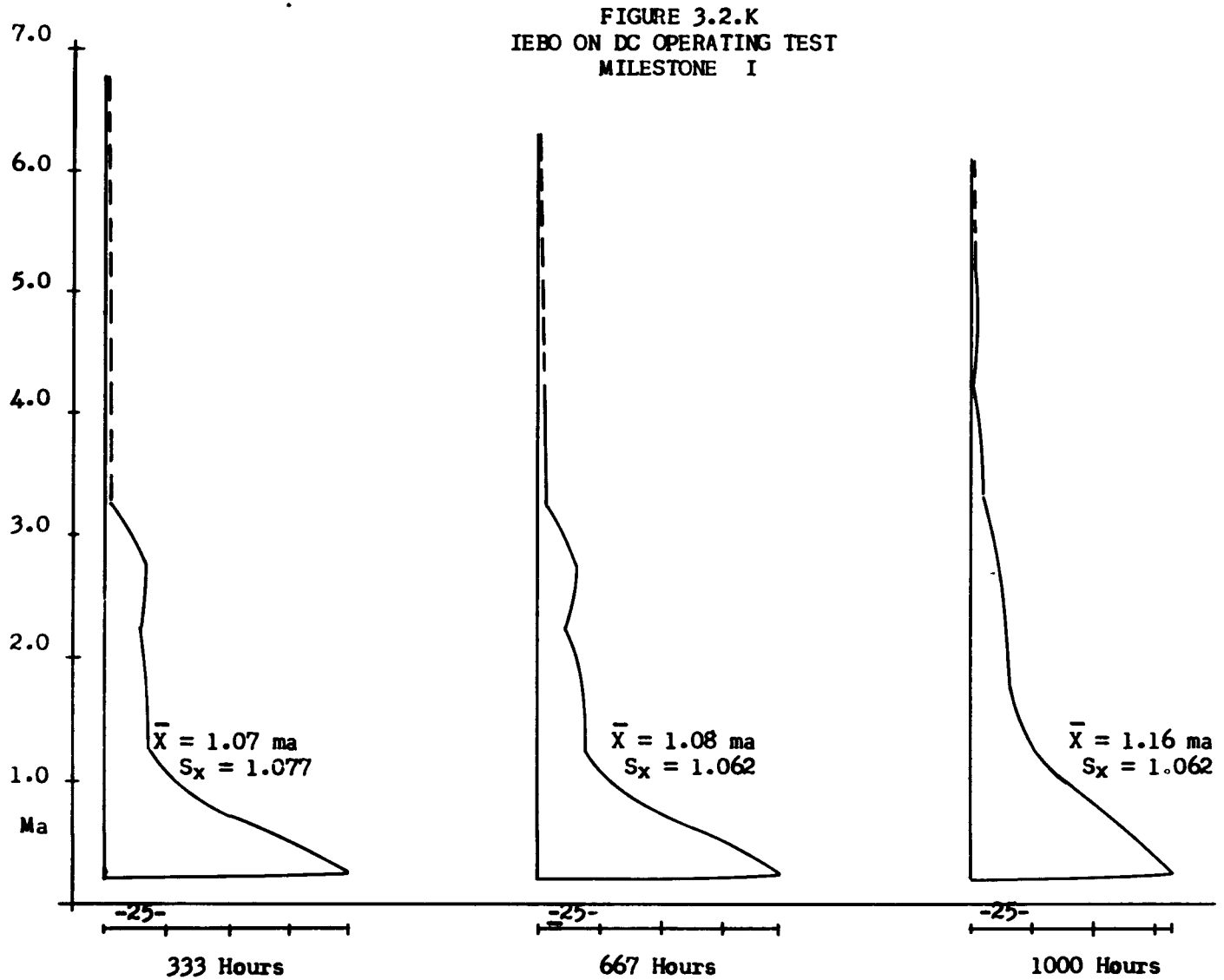
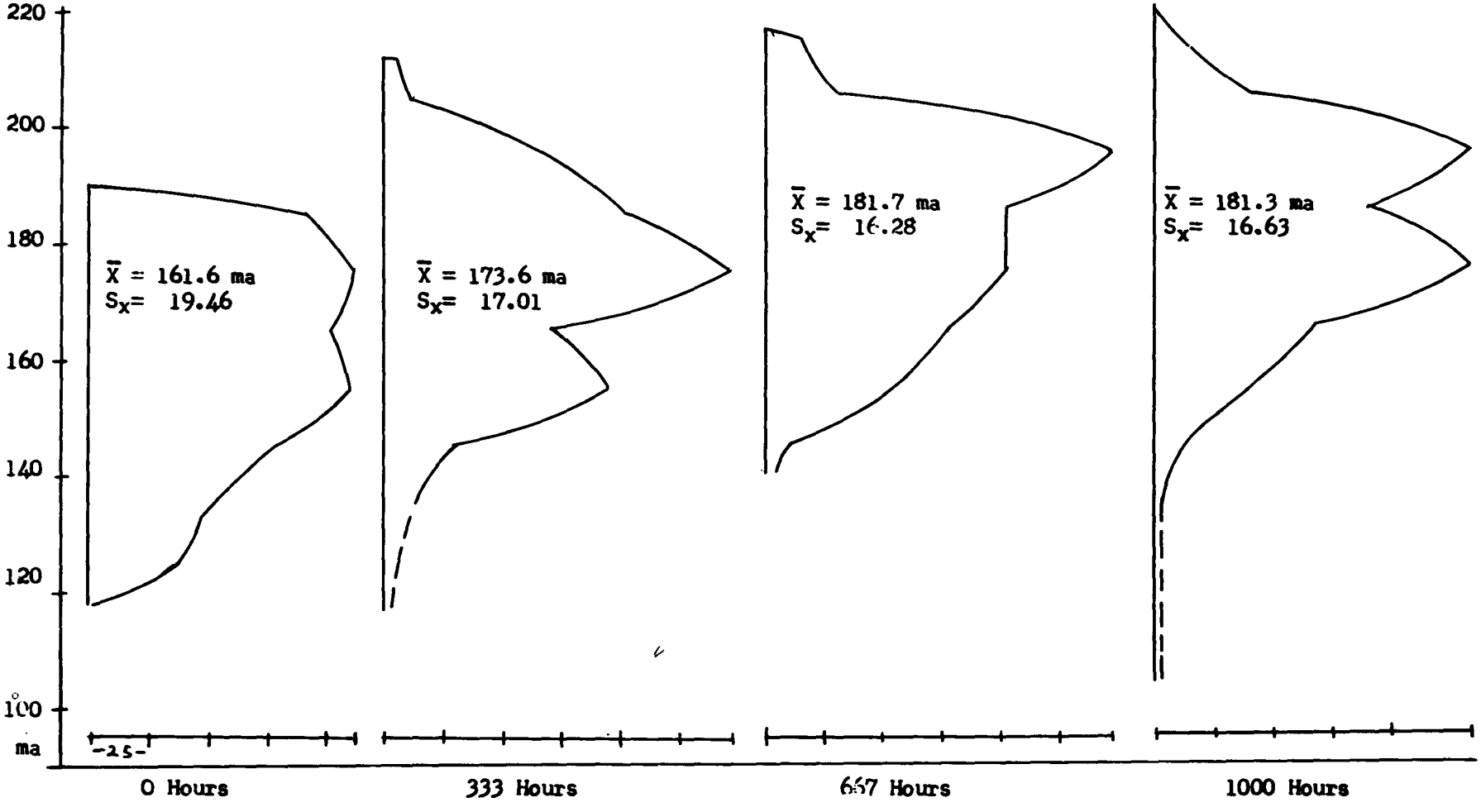


FIGURE 3.2.L
JB_2 ON DC OPERATING TEST
MILESTONE I



that T_j = 100°C at 20 watts is considerably less severe than T_A = 135°C at zero watts in terms of ICBO stability. IEBO was again better with a mean shift of only .09ma to a final value of 1.16ma. IB_2 was much like storage only less extreme: 20.1ma mean shift, initial to 666; tightened dispersion (S_x = 19.46 to S_x = 16.63, initial to 1000 hours).

The manufacture of Milestone Lot I was closely monitored and documented. Every attempt was made to follow the normal production flow. The over-all yield was higher than production lots on either side, as shown on Figure 3-2-M (Lot 44). The reliability of the raw production lot was in line with the then present trend, as shown by manufacturing control results (Figure 3-2-N). Of the 17 process improvement items in the contract, 3 were in effect. The Milestone units were I.D. sawed (3.1.2); wafer flash etched (3.1.7); and the base preparation was in a hydrogen atmosphere (3.1.12). The lot was begun June 28, 1962, and mounted for test August 25, 1962. The production of Milestone II devices is nearly complete and Milestone III has begun.

The failure mechanisms observed and the Milestone I manufacturing control testing are discussed in Sections 3.3 and 3.2.2, respectively.

Conclusions. Neither Milestone I storage nor D.C. operating levels were achieved. The failure rates at 90% confidence were 6.99 and 7.93% per 1000 hours, respectively. Units for Milestone II are nearly ready for testing and Milestone III units are in production.

Program for the Next Quarter. Milestone Test II will be completed and Milestone III will be placed on test.

3.2.2 Manufacturing Control Reliability Tests - D. J. Lindgren.

General. Procedures for evaluating daily samples from the transistor production line at 135°C have remained the same during this second quarter. Figures 3-2-M and 3-2-N show the normalized yield after 112 hours at 110°C, and normalized cumulative percent failed to 1000 hours at 135°C, respectively. Due to the wide variation between lots, it is deemed advisable to use at least 50 lots as the base-line from which quarterly differences will be noted. Thus, using a total of 58 lots, the base-line is established.

Prior to the receipt of this contract, an experiment was conducted to evaluate existing capabilities of the transistor at 135°C. This department accumulated raw samples from production into weekly lots of 100 pieces. Storage and testing procedures were very similar to those used in present evaluations. Subsequently, the Engineering Department sampled units which had come from the same week's population (as evidenced by cap date codes); the only difference being that Engineering sampled from these lots after they had been through Inspection and Quality Control tests. Figure 3-2-O shows how the screening tests of those departments affected subsequent failure levels at 135°C. The same comparison is also shown on this graph for Milestone Lot No. 1, whose life distribution was predicted on the basis of the sample from the Milestone lot, even before Milestone Lot I had reached its first readout.

FIGURE 3.2.M
MFG. CONTROL DAILY SAMPLING FOR 135°C STORAGE
NORMALIZED YIELD Vs. LOT NO.

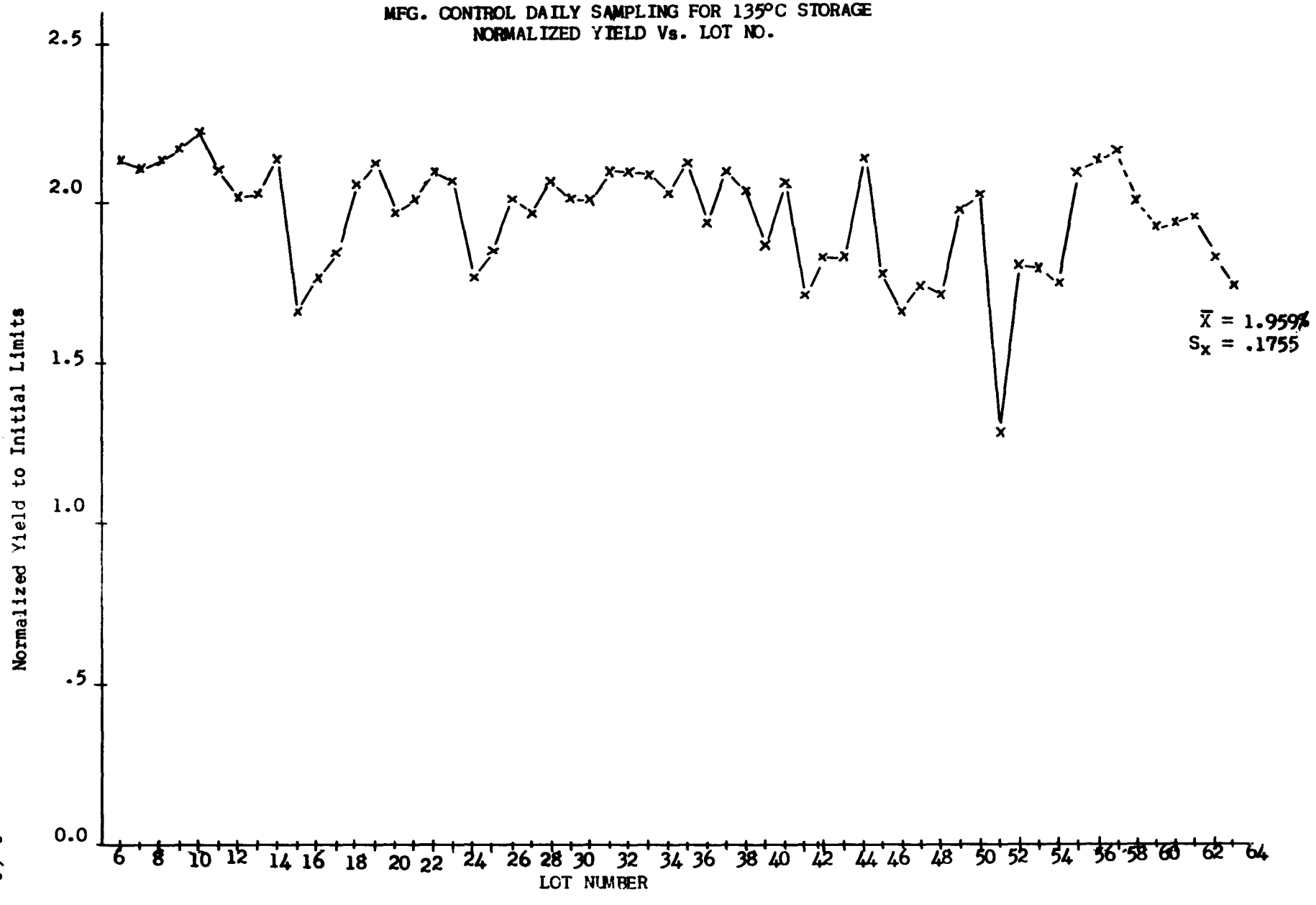


FIGURE 3.2.N
MFG. CONTROL DAILY SAMPLING FOR 135°C STORAGE
NORMALIZED CUMULATIVE PERCENT FAILED
Vs.
Lot Number
N = 50 Per Day After 1000 Hours

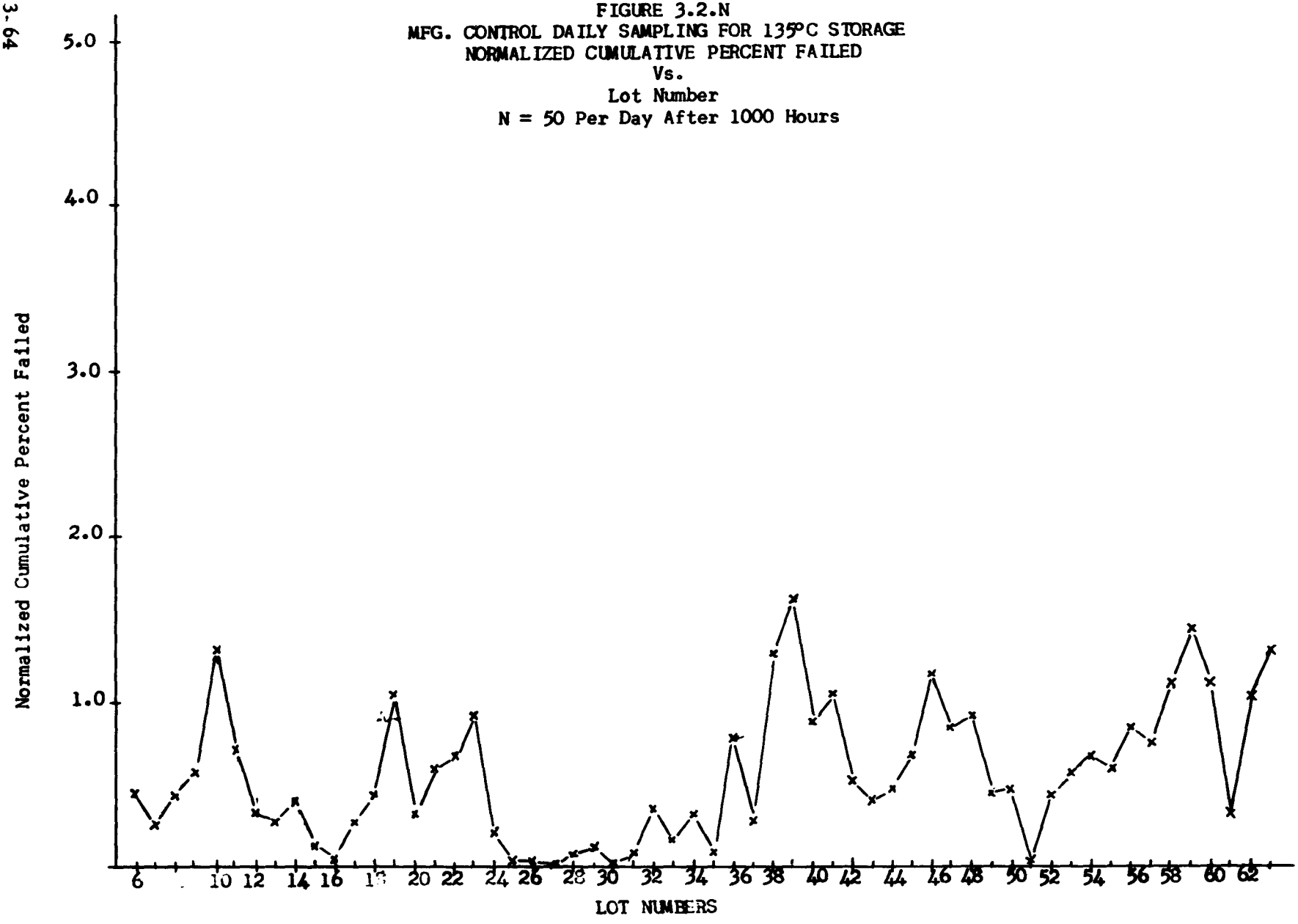
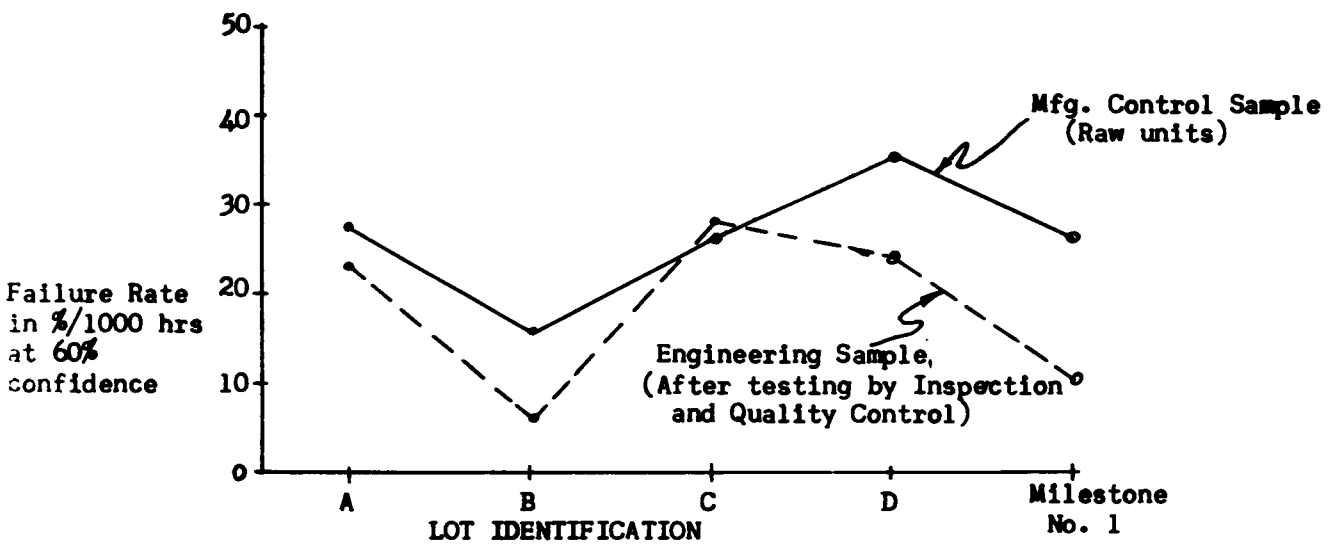


FIGURE 3.2.0
MANUFACTURING CONTROL SAMPLES
Vs.
ENGINEERING SAMPLES
AFTER 1000 HOURS AT 135°C
(Note: All rates are computed using Mfg. Control Limits)



Two of the earliest of these experimental lots (run before receipt of the contract) are still on test, and have completed 5000 hours at 135°C. Figure 3 2-P shows how they have performed during this time, giving an indication how relatively unhelpful a "burn-in" period would be in reducing failure rate.

One of the most variable factors in production has been the depth of electrolytic etching. It has been theorized that this contributes to the failure of a transistor at 135°C. Therefore, an experimental group of transistors was subjected to a considerably lighter etch. After encapsulation, they were evaluated in the usual manner at 135°C, along with a group of normally etched transistors. The results are shown in Figure 3-2-Q. Conclusions are indecisive, however, since the magnitude of variation is small between the groups. The difference in etching tried was expected to produce a relatively small, but detectable, variation in reliability. Since both the control and experimental groups exhibited substantial failures, some additional mechanism appears to have masked the effect of the etching change. It is planned that the experiment be repeated on low failure rate material.

Conclusions. Lot-to-lot variation remains very large. Obviously, this variation must be reduced, as well as the level of failures, if our goal is to be attained. Thus, earlier indicators of poor lots must be discovered in order that production difficulties may be corrected.

Observation of Figure 3-2-P, showing the performance of two early lots stored 5000 hours at 135°C, indicates that a "burn-in" period would not reduce failure rate, assuming, of course, that these two lots are typical.

FIGURE 3.2.P
MFG. CONTROL EXTENDED TESTING

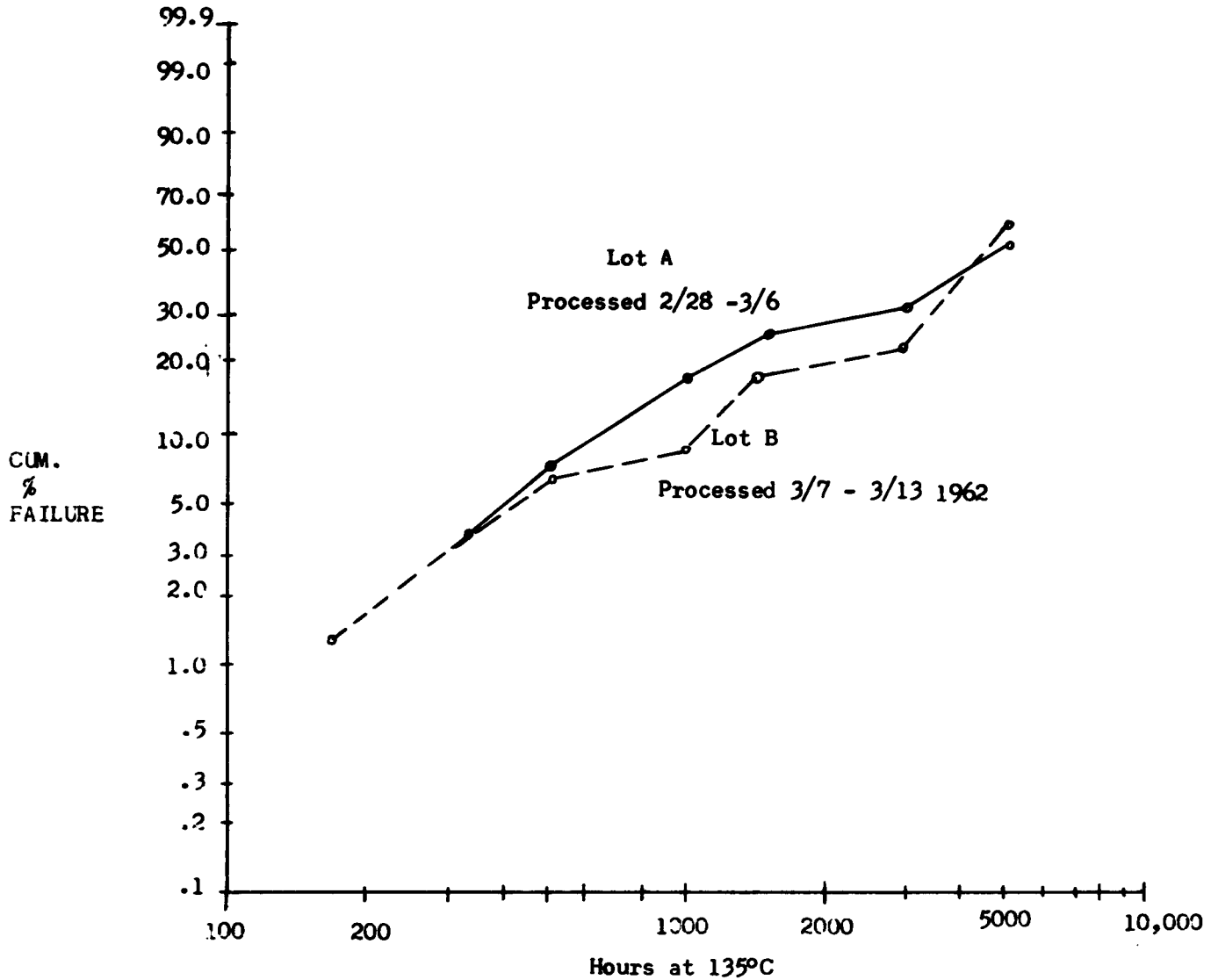
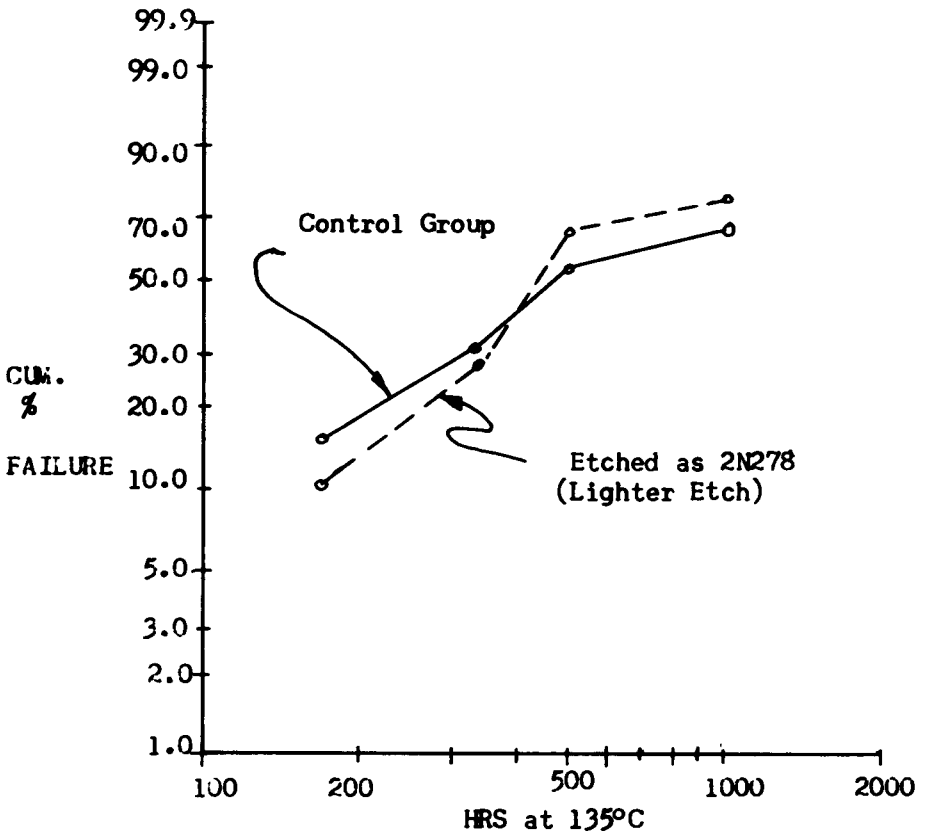


FIGURE 3.2.Q
MFG. CONTROL EXPERIMENT



The performance of lot number 51 suggests that high yields and high reliability do not necessarily go together. Also, implied by this result is that certain conditions causing low gain lead to high reliability.

Program for the Next Quarter. Manufacturing Control will relocate at the new Manufacturing Building, along with the final assembly area. Daily samples will continue to be evaluated, and attempts to correlate results with those of Milestone lots will likewise continue. Attempts will be made, using data from completed lots, to relate final results to data taken in the early stages of testing, in order to sound an alarm to production at a time early enough that difficulties may be located and corrected. With the same purpose in mind, cooperation with Engineering in establishing correlations between usual 135°C tests and step-stress tests will be maintained. The data collection for a computor run multiple regression study is nearing completion. Initial parameter means and first and second week parameter shifts will be correlated with failure rate.

3.2.3 Special Reliability Experiments - L. V. Ingle.

General. The first of four 600 watt pulse life experiments has been completed. The 40 units were selected from the same production lot as Milestone I. Although test points occurred only at 500 and 1000 hours, the time of failure was observed in the lighted control panel. It is interesting to note that a "good" fit was obtained with the failure data which yielded a Weibull slope of 1.3. This relationship was particularly evident between 90 and

600 hours where nearly all the plotted points fell close to the line (Figure 3-2-R). The 600 watt pulse condition was chosen because it was the most accelerated of the Minuteman pulse conditions, and it created a unique failure mode.

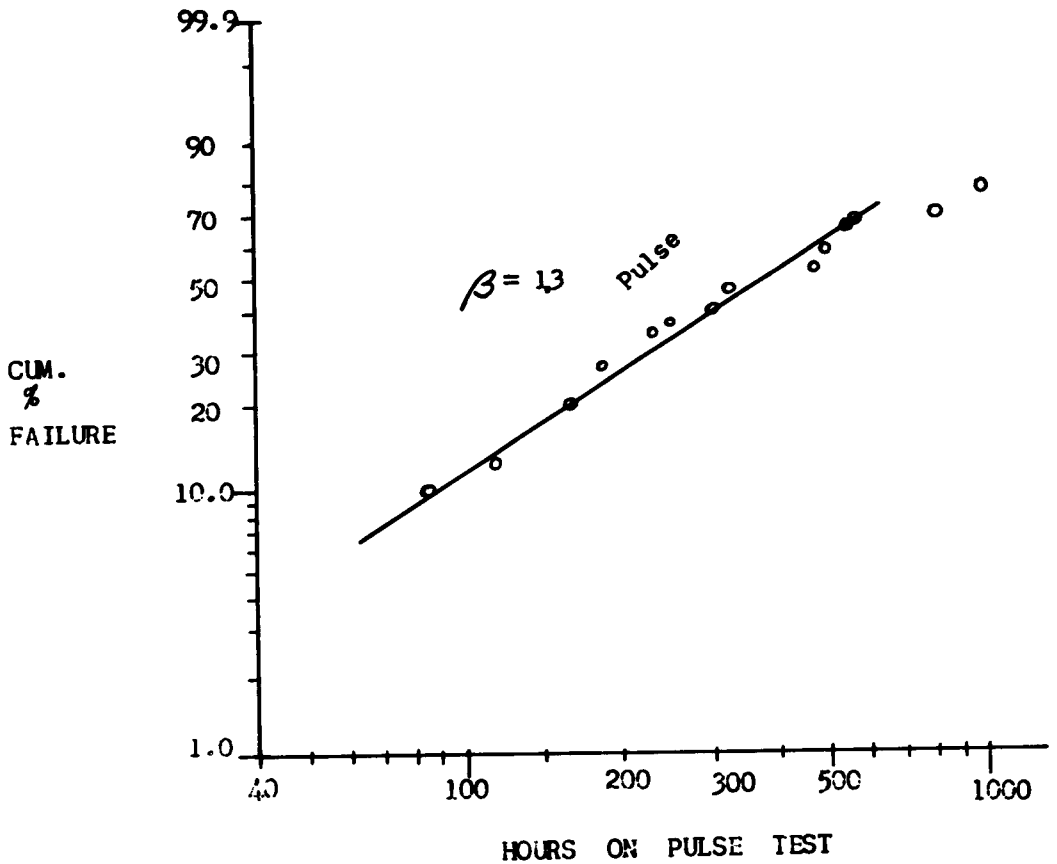
The failure is ultimately produced by the creepage of indium as it cycles from liquid to solid states with the 600 watt pulses. Complete analysis of the failed devices is contained in the Failure Analysis Section of this report.

Thirty-one of the forty units failed during the 1000 hour test. Parameter distributions are not shown because (1) the nine good units' parameters were relatively unchanged during the test; and (2) it was not possible to obtain parameter readings on the 31 destroyed devices.

Step-Stress Experiments. The immediate objective of the efforts in this area is to develop a three step testing procedure for quickly evaluating daily production and process changes. The amount of time and units will increase with each phase, while the temperature will decrease. The first step will require approximately 25 units for 18 hours. The accept-reject limits will be broad, but exceptionally good or poor material should be detectable. If acceptable or questionable, a second sample of 50 to 100 units will be placed on accelerated storage for one week. If still favorable, a larger proof group will be placed at 135°C for 1000 hours. If the testing proves successful, the savings in material, labor, and decision making time are obvious.

Two separate step-stress experiments have been completed during the 2nd quarter. The first group consisted of 150 units

FIGURE 3.2.R
PULSE FAILURE DISTRIBUTION
MILESTONE I



selected from raw production and were required to have VCBO $\geq$ 80V at IC = 4ma only. Three equal groups were then subjected to ascending thermal steps for .5, 3, and 18 hour intervals, respectively. VCBO and VEBO at IC = 4ma and IB_2 (VCE = -2V, IC = 5ma) were read out after each step. The steps began at 127° and progressed to the oven maximum of 282°C. The individual increases in temperature were -5×10^{-5} reciprocal degrees Kelvin which is approximately 10°C at 200°C. The second group of units was chosen from production with Lot No. 70, as shown in the Manufacturing Control section. Thus, Lot 70, which will undergo the customary 1000 hours at 135°C, will be used as a base line from which to develop acceleration relationships. In addition, units from the same group were placed on 158°C storage. The parameters monitored were the same as those for manufacturing control and Milestone Tests (ICBO, IEBO, and IB_2).

With failure limits initially fixed at VCBO, VEBO $\leq$ 20V, the relationships shown by Figure 3-2-S were obtained. It is apparent that the predicted temperature relationship is present and the effects of time are clearly defined. It is further evident that linearity is best between 20% and 80% failed. As further evidence, the lower line was obtained on a diamond base Delco power transistor under reverse biasing conditions by an independent agency. The 50% failure points are as follows:

.5 hour/step ---- 275°C
3 hour/step ---- 235°C
18 hour/step ---- 195°C

This reveals the first approximation of the time-temperature conditions: six times step time yields the same percent failure as a 40°C increase in temperature.

FIGURE 3.2.S
AMBIENT TEMPERATURE STEP STRESS EXPERIMENT
VCBO 20V FAILURE LIMIT

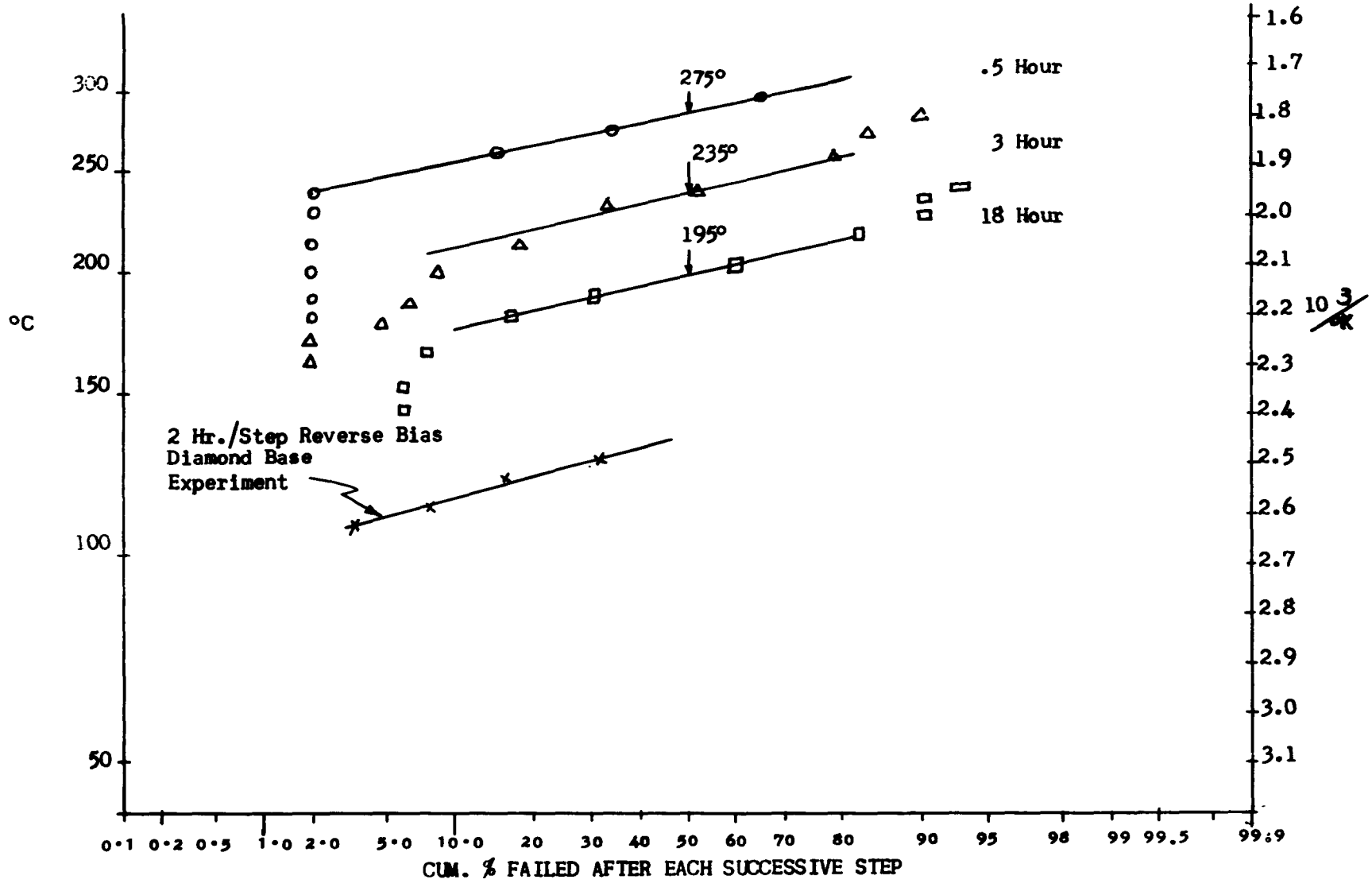


Figure 3-2-T shows the behavior of mean VCBO with temperature. The linearity of the semilogarithmic plot suggests an Eyring model of the form:

$$R = C\, e^{-b/T}$$

where b is the ratio of the activation energy to Boltzmann's constant, b = E/K, and R is the time rate of movement from "good" to "bad."

Although all three time constant slopes appear to be approximately parallel, the 18 hour line was selected for evaluation and further usage. Within the range of readily available temperature, it offered the most points and best defined the complete transition. The activation energy as calculated between 1.90 and 2.20 (10^3 /T reciprocal °K) is .24 e.v. for VCBO. The associated E for VEBO as shown by Figure 3-2-U is .17 e.v. This is the reason there are more collector failures than emitter on conventional life test; the degradation is both swifter and more severe.

The upturn shown by VCBO and VEBO is believed to be related to the IC versus t phenomenon discussed in Section 3.4.1 concerning degraded units. The discussion, as presented there, is believed to apply because (1) an automatic digital readout test set with a fixed testing time (t) of 65 milliseconds was used throughout the test; and (2) the "recovering" devices all exhibited looped degraded traces when received by Failure Analysis. Thus, it appears that the automatic test set began to sample on the "up" side of the peak leakage (low voltage) after the units degraded below a certain level. This improvement is also not

FIGURE 3.2.T
LOG VCBO MEAN Vs. 1/T

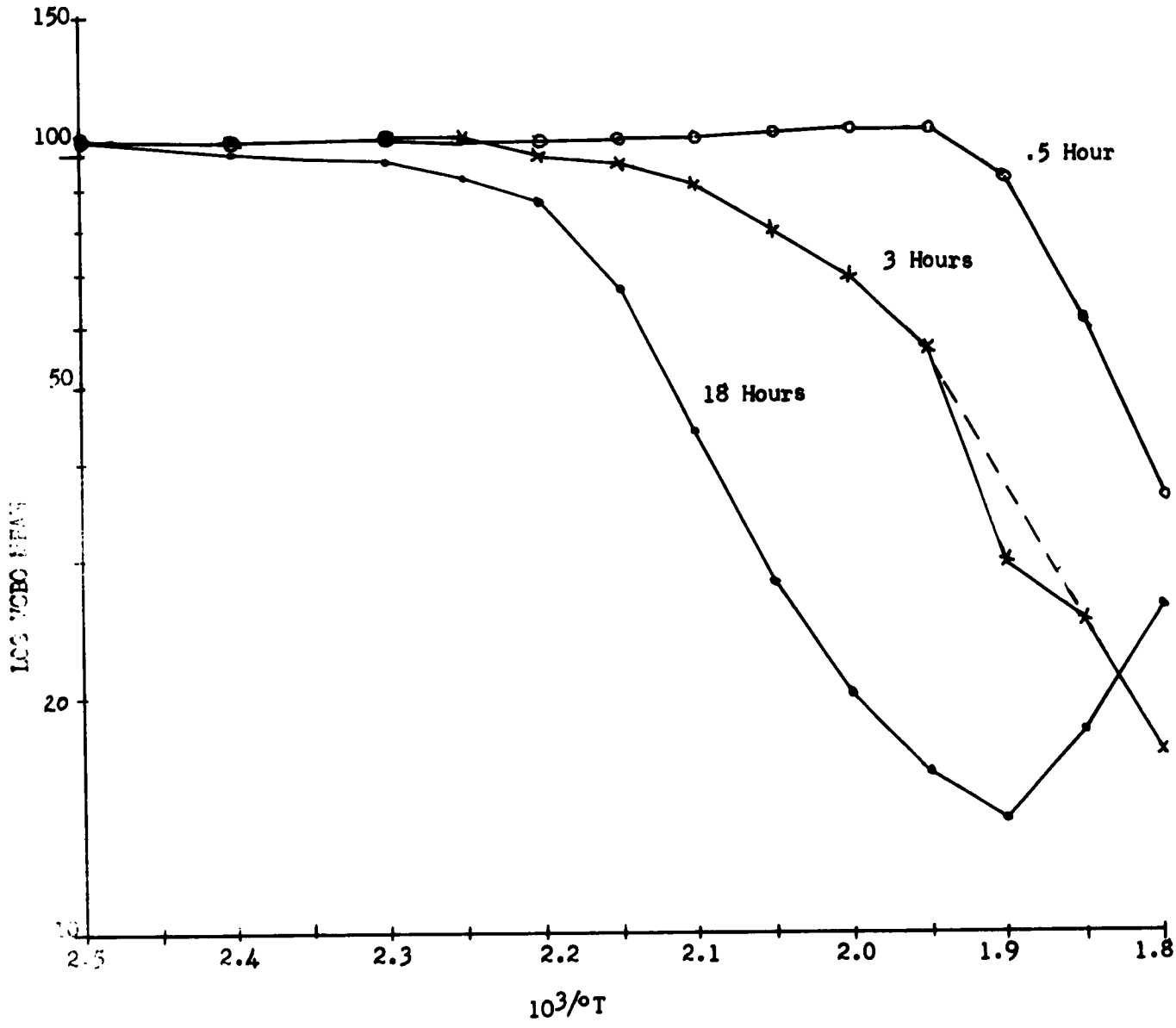
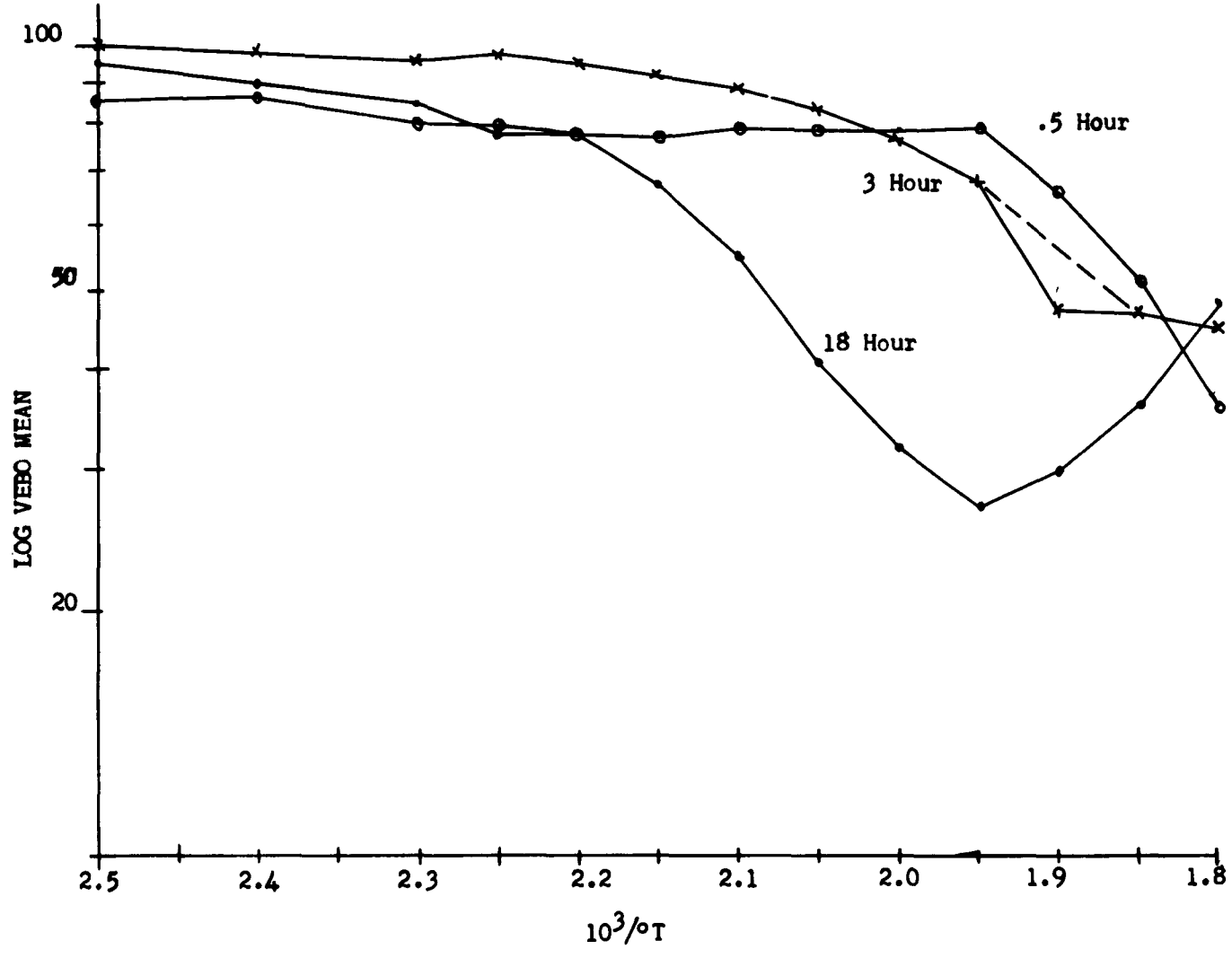


FIGURE 3.2.U
LOG VEBO MEAN Vs. 1/T



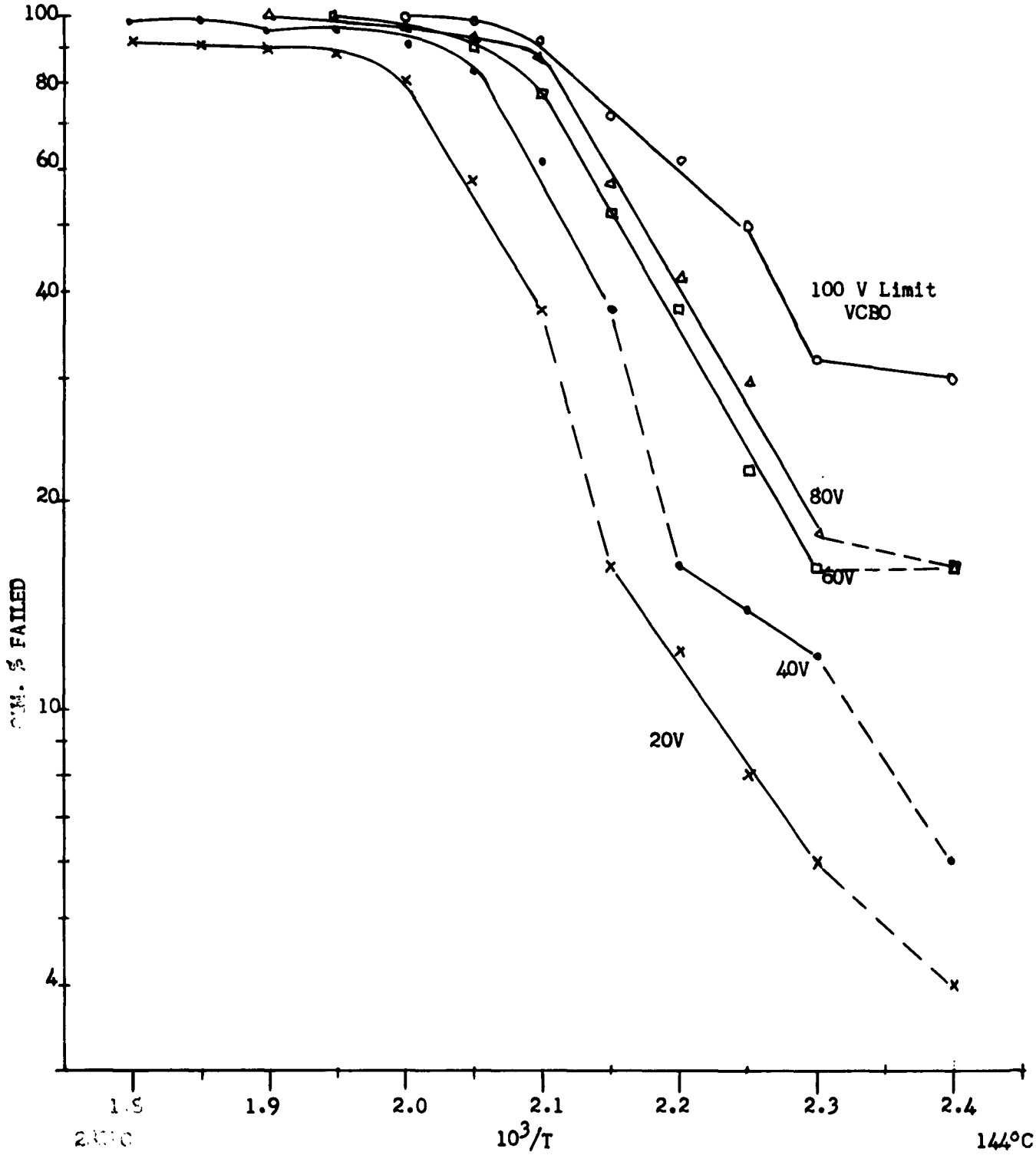
present on the meter read current experiment conducted under the same conditions.

Another "R" available for discussion is the cumulative percent failed to various end points. The resultant 18 hour curves are shown by Figure 3-2-V for VCBO$\leq$20, 40, 60, 80, and 100V limits. Linearity was best achieved for 60 and 80V, and the fitted lines are shown on Figure 3-2-W. E was calculated as .30 e.v. The compliment treatment of VEBO (Figures 3-2-X and 3-2-Y) yielded E $\sim$ .26 e.v.

The second experiment was conducted on 110 units from manufacturing control lot No. 70. Two groups of 25 units each were step-stressed as described above at 3 and 18 hour time intervals. Twenty units were placed at 158°C storage, and forty were used for four one-shot checks on the step-stress lines. The units met the initial requirements for manufacturing control and IC, IE, and IB_2 were monitored at readout points. Figure 3-2-Z displays the failure distribution versus $10^3/°K$. for 10ma. diode leakage end points. Linearity is evident between 30 and 90% failed with the 50% failure temperatures occurring at 214°C for 18 hour, and 238°C for 3 hour steps. Thus, for 10ma failure limits, six times the step-time gives the same result as increasing the step temperature 24°C. For 25ma end points, the difference is 20°C.

Figure 3-2-AA is a plot of log percent failed versus $10^3/T$ for various end points of ICBO. Linearity was again noted with the 10ma, 20ma, and 25ma lines chosen for regression analysis. The respective E's calculated and shown on Figure 3-2-BB are .36 e.v., .28 e.v., and .45 e.v. These results, though none of them is the exact .30 shown for VCBO end points,

FIGURE 3.2V
18 Hr. Steps - VCBO Limit Only
CUM. % FAILED Vs. 1/T



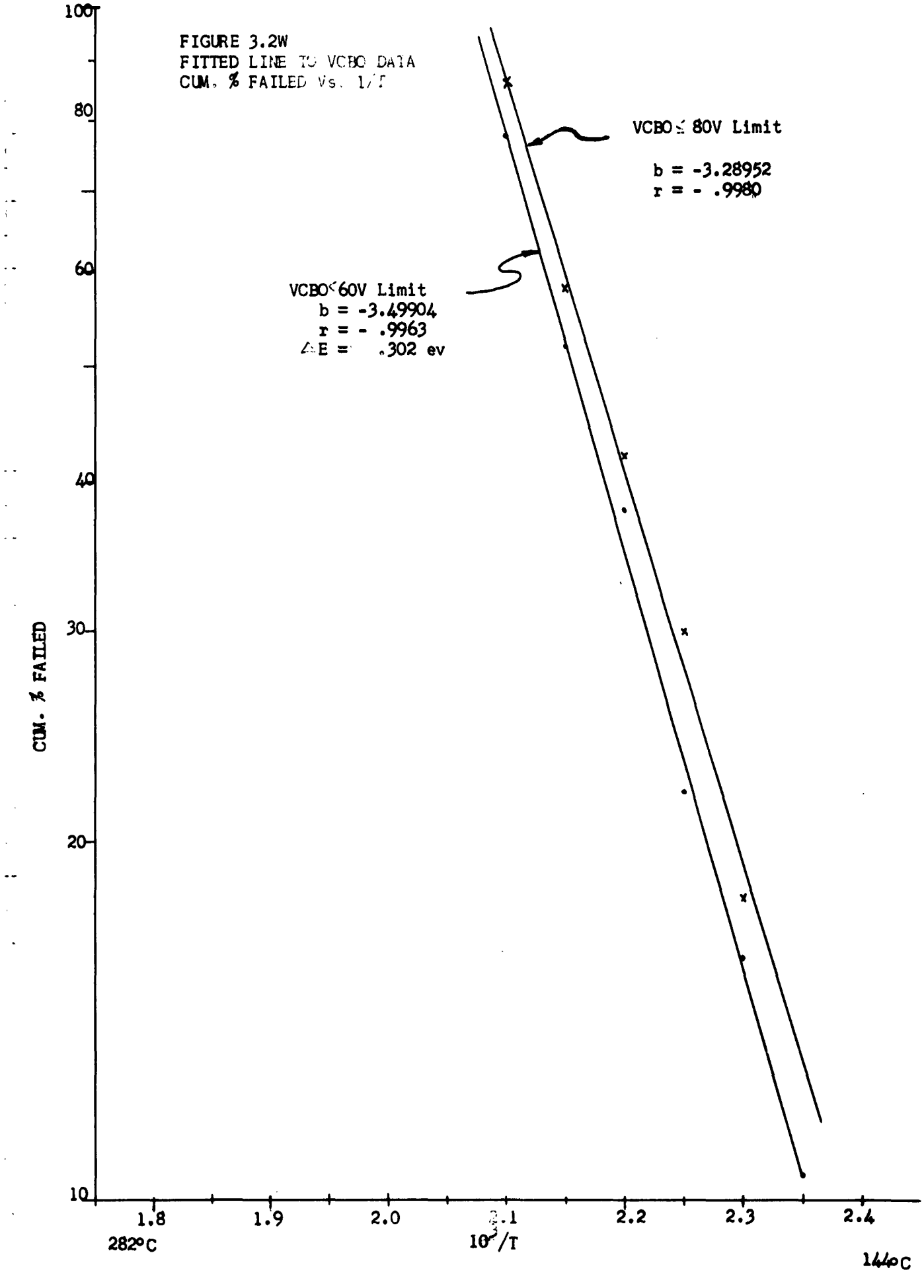


FIGURE 3.2W
FITTED LINE TO VCBO DATA
CUM. % FAILED Vs. 1/T
VCBO ≤ 80V Limit
b = -3.28952
r = - .9980
VCBO < 60V Limit
b = -3.49904
r = - .9963
ΔE = .302 ev
CUM. % FAILED
100
80
60
40
30
20
10
1.8
1.9
2.0
2.1
2.2
2.3
2.4
282°C
10⁴/T
144°C

VEBO FAILURES TO FOUR END POINTS
FIGURE 3.2.X

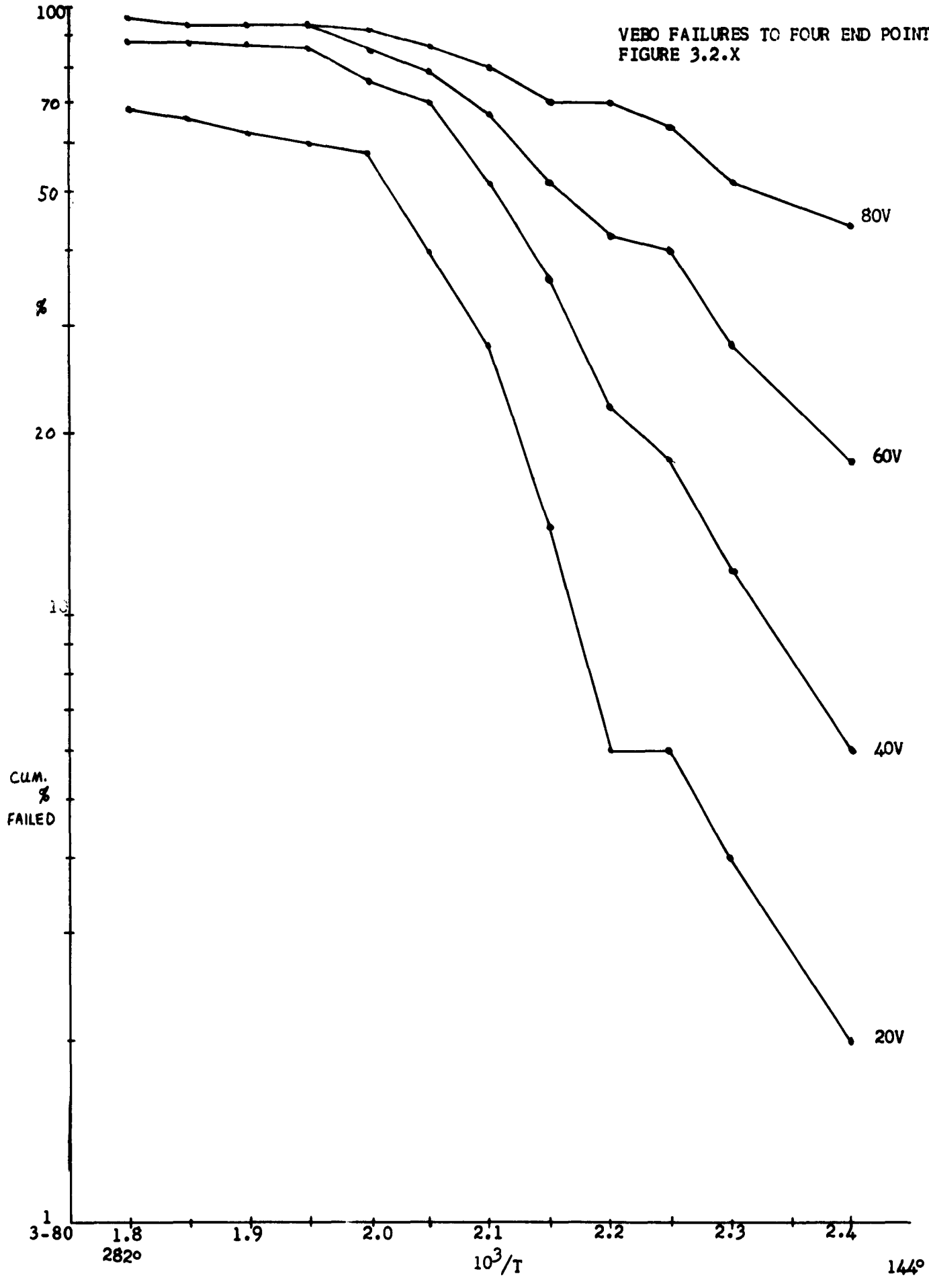


FIGURE 3.2.Y
REGRESSION LINE FOR VEBO

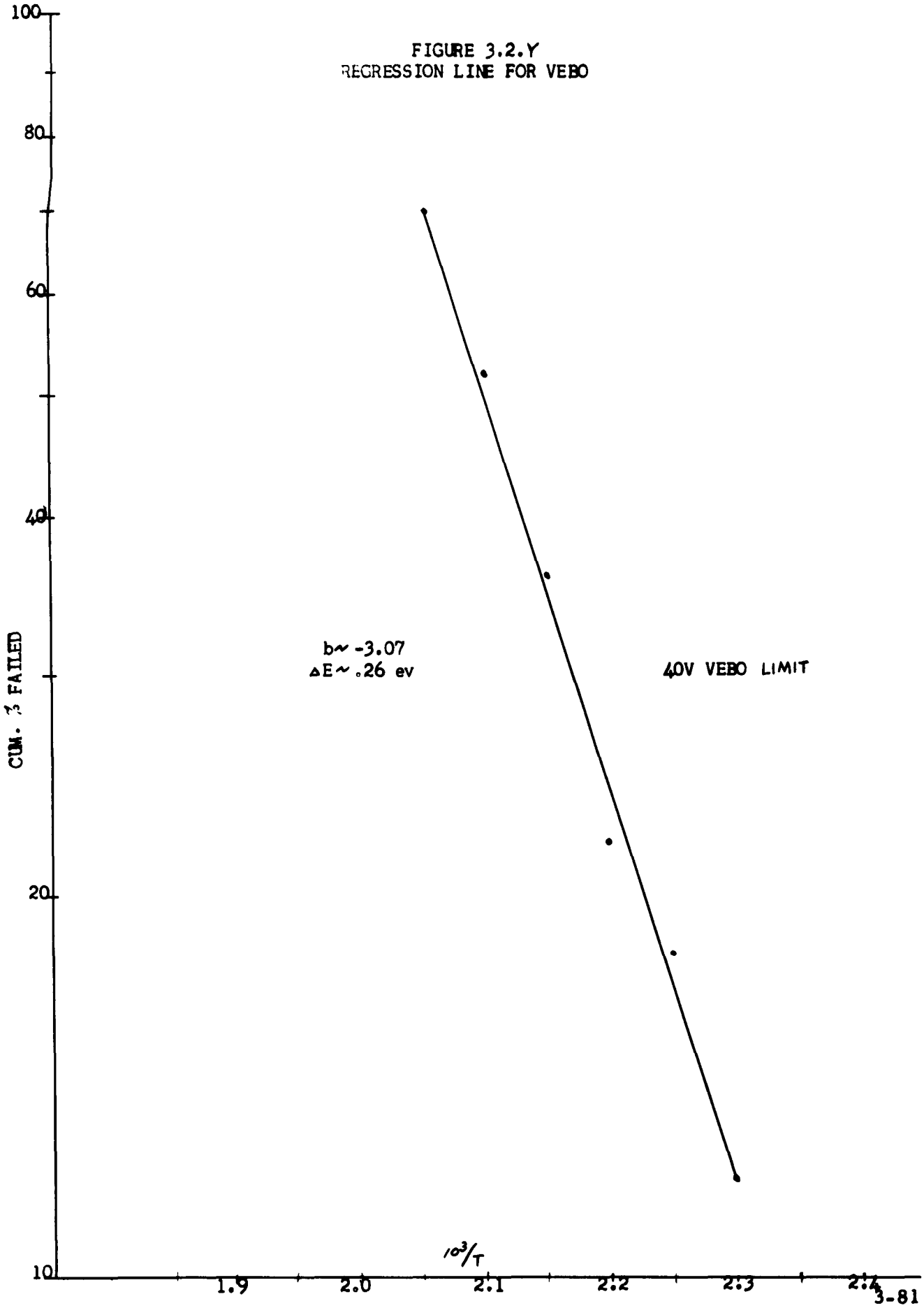


FIGURE 3.2.Z
FAILURE PATTERNS FOR I_C, I_E > 10 Ma

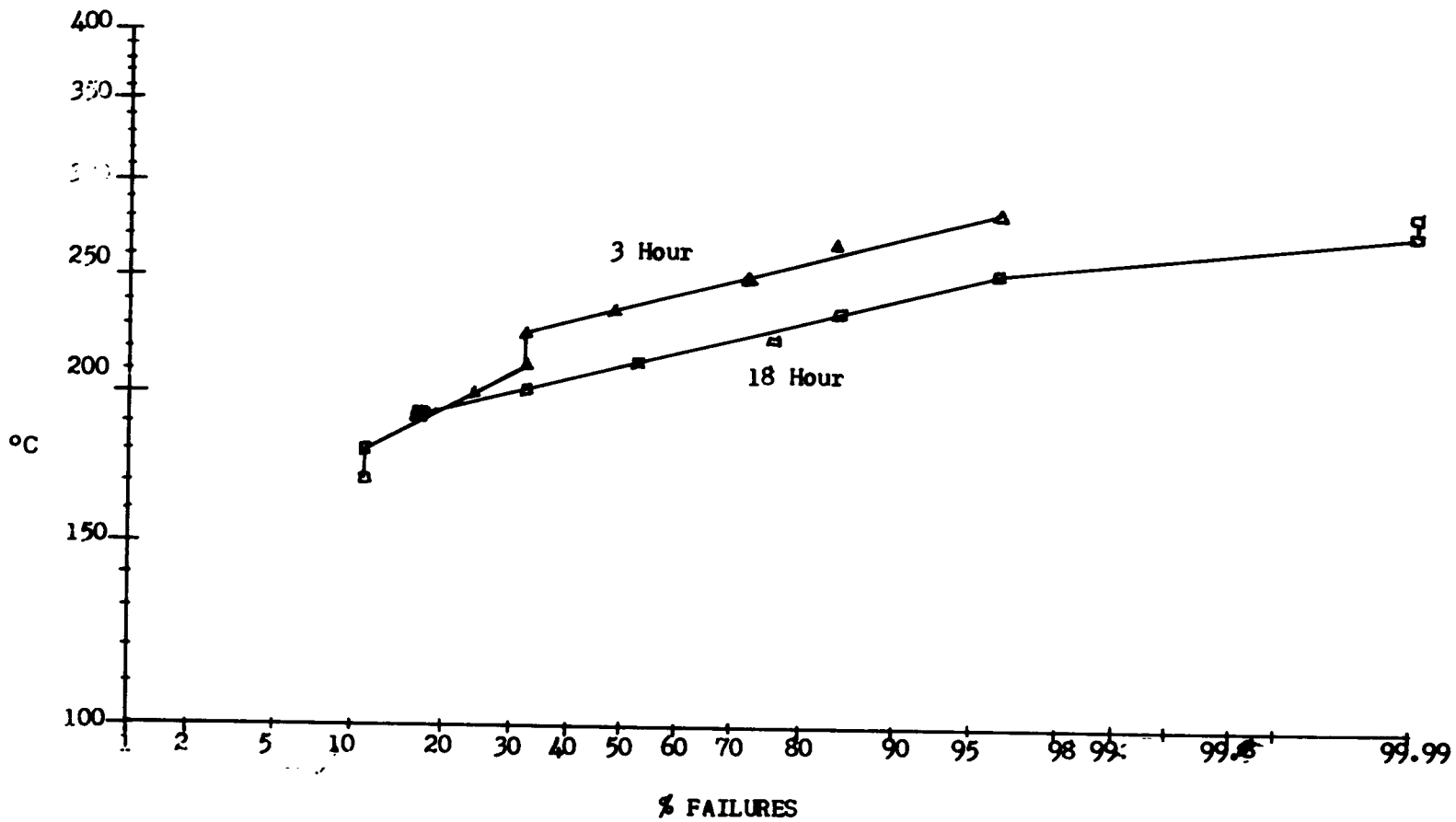


FIGURE 3.2.AA
18 HRS. STEP STRESS-ICBO

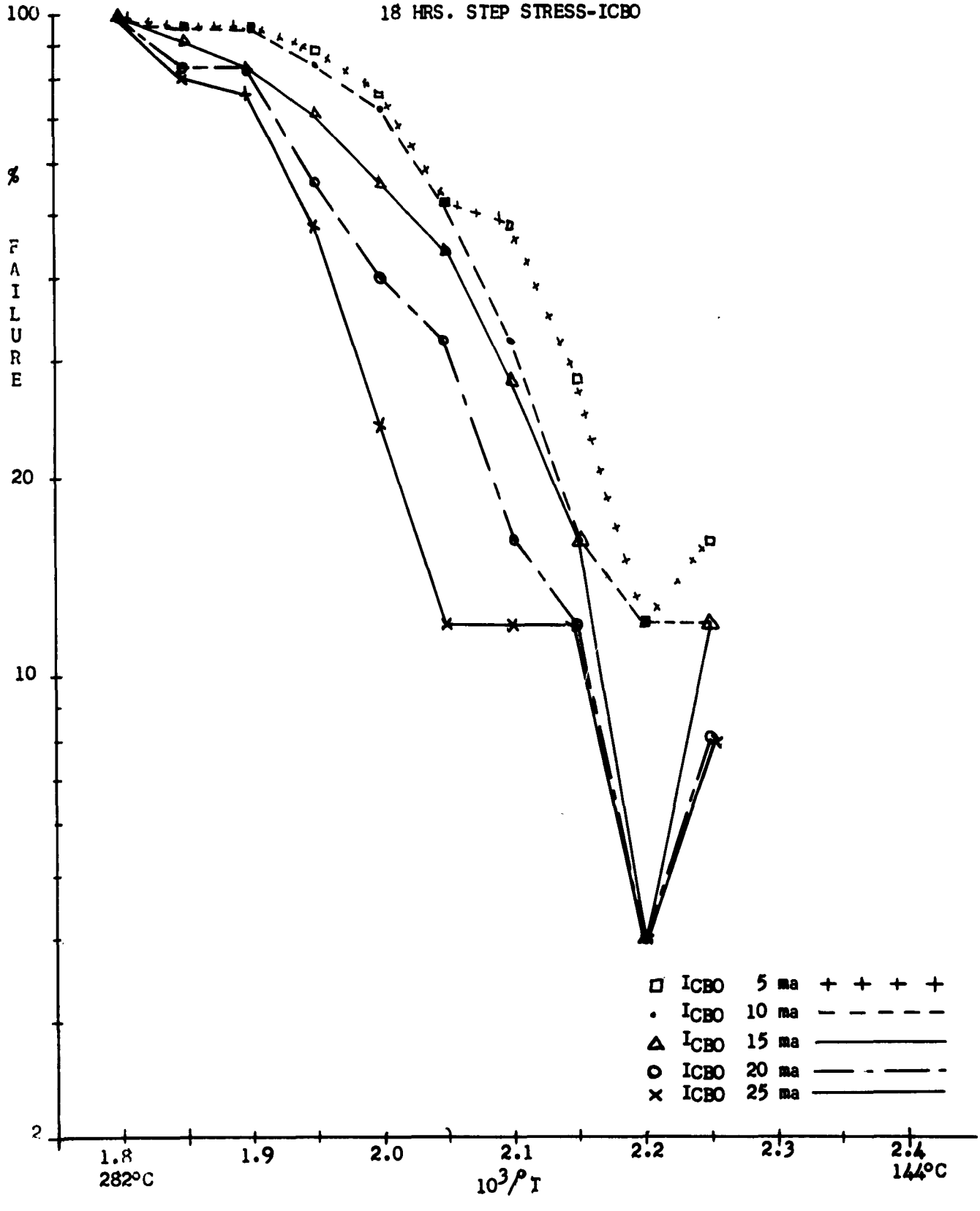
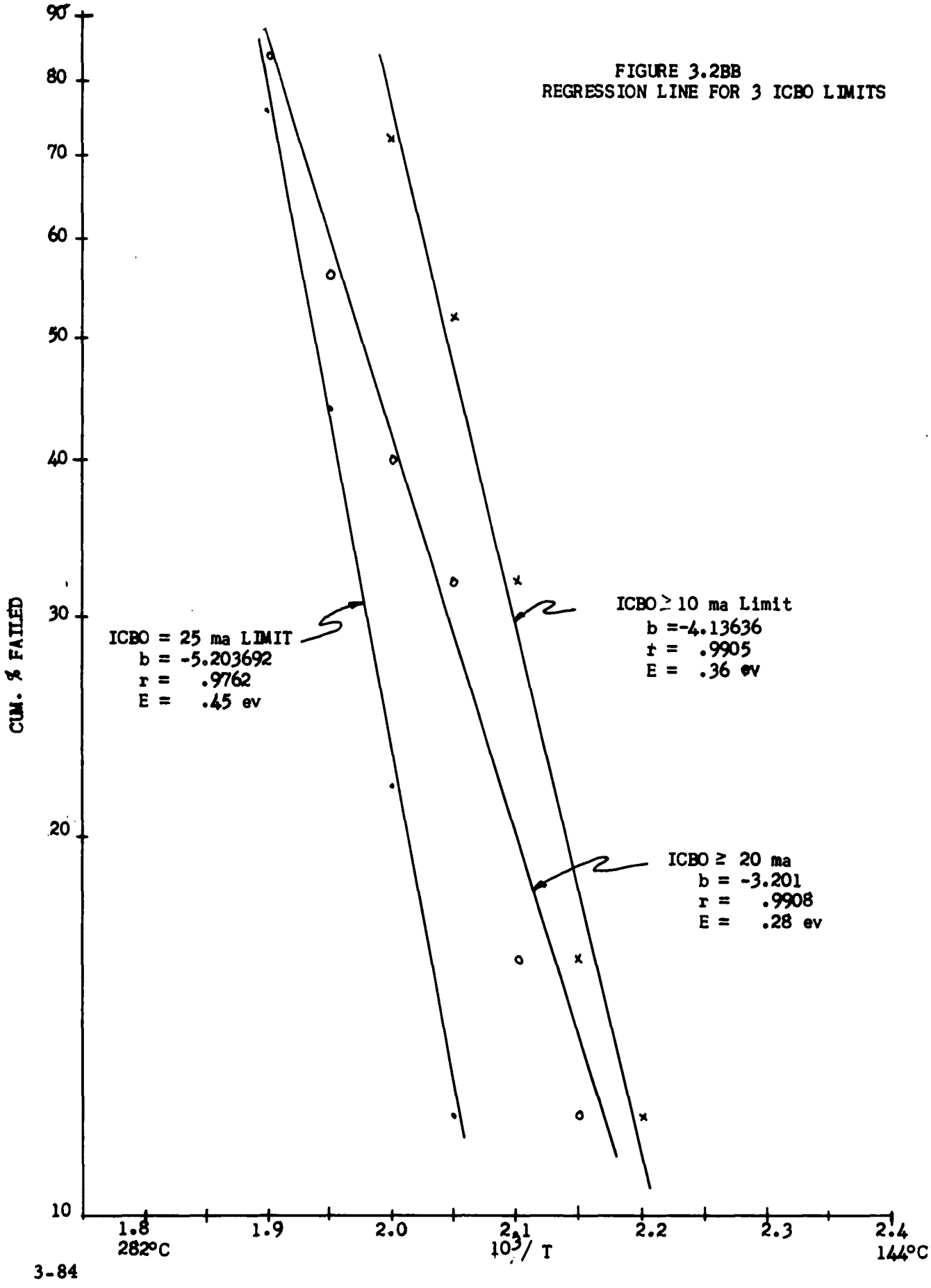


FIGURE 3.2BB
REGRESSION LINE FOR 3 ICBO LIMITS



show that the same form of activation was present in both groups and ICBO - VCBO failure endpoints are comparable.

A semilogarithmic plot of ICBO mean at the 18 hour interval is shown by Figure 3-2-CC. The temperature dependency is again apparent with calculated E between 181°C and 252°C being .24 e.v. Similar analysis of Figure 3-2-DD of IEBO mean yields E= .23 e.v. The same parameters at the 3 hour intervals were E_{ICBO} = .31 e.v., and E_{IEBO} = 2.1 e.v. (Figures 3-2-EE and 3-2-FF).

Four groups of ten units each were used to test the initial assumption that prior aging does not affect the time of failure. The appropriate °C for 35% and 65% failed were taken graphically from Figure 3-2-Z for both 3 and 18 hours.

	35%		65%	
	225°C	202°C	243°C	220°C
3 hr.	20%	-	90%	-
18 hr.	-	30%	-	40%

The results, as shown in the table above, were somewhat discouraging at first. The only point of verification appeared to be the 30% attained at 202°C. The over-all acceptance criteria was set at (2 x 3.5 + 2 x 6.5) 20 ± 2 failed units out of 40, and 18 failures were observed; therefore, the lack of individual acceptance may be due to small sample sizes. Further attempts with future groups will be conducted with larger sample sizes and repetitious comparison.

FIGURE 3.2.CC
LOG ICBO MEAN 18 HRS

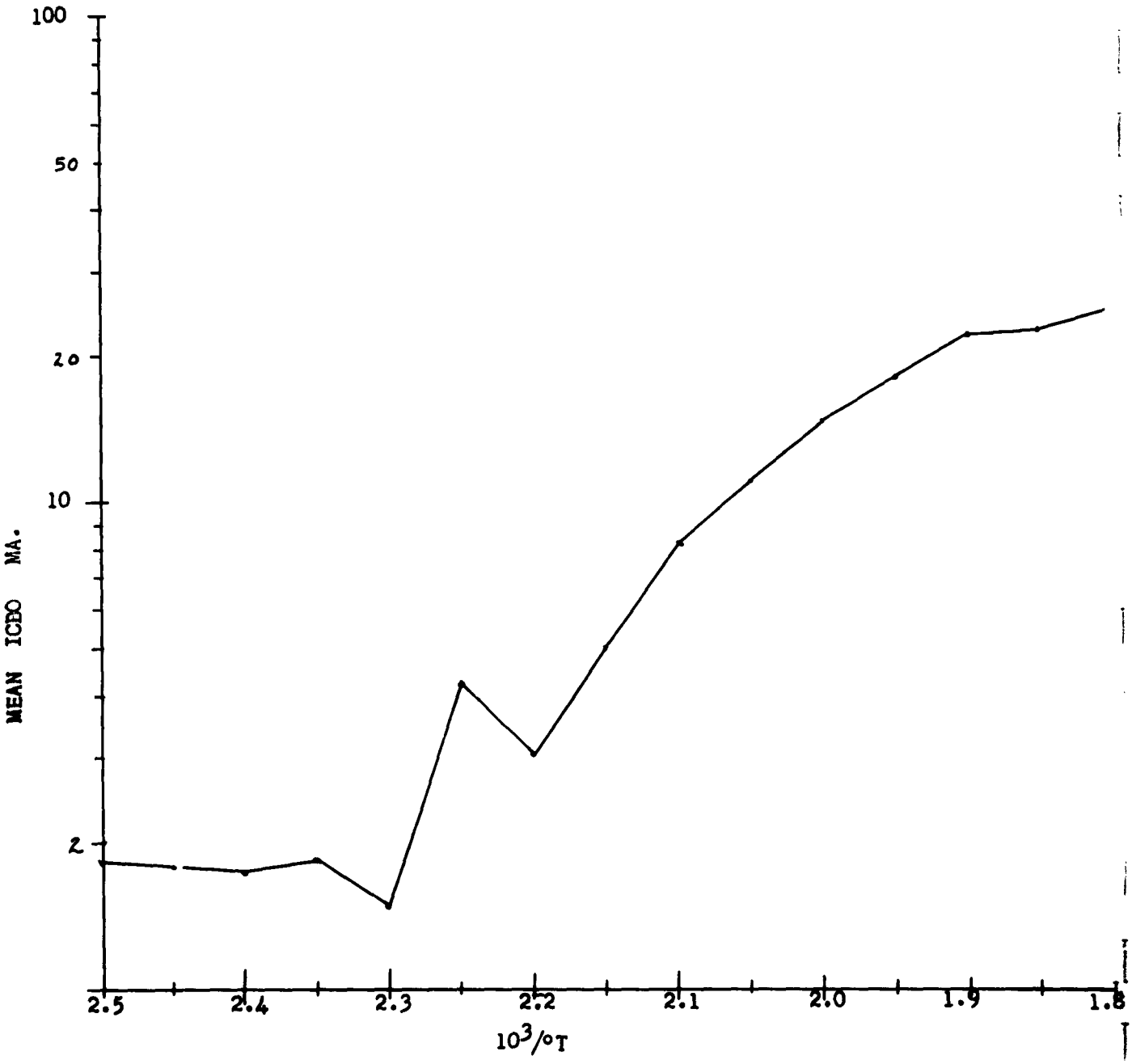


FIGURE 3.2.DD
LOG IEBO MEAN 18 HRS

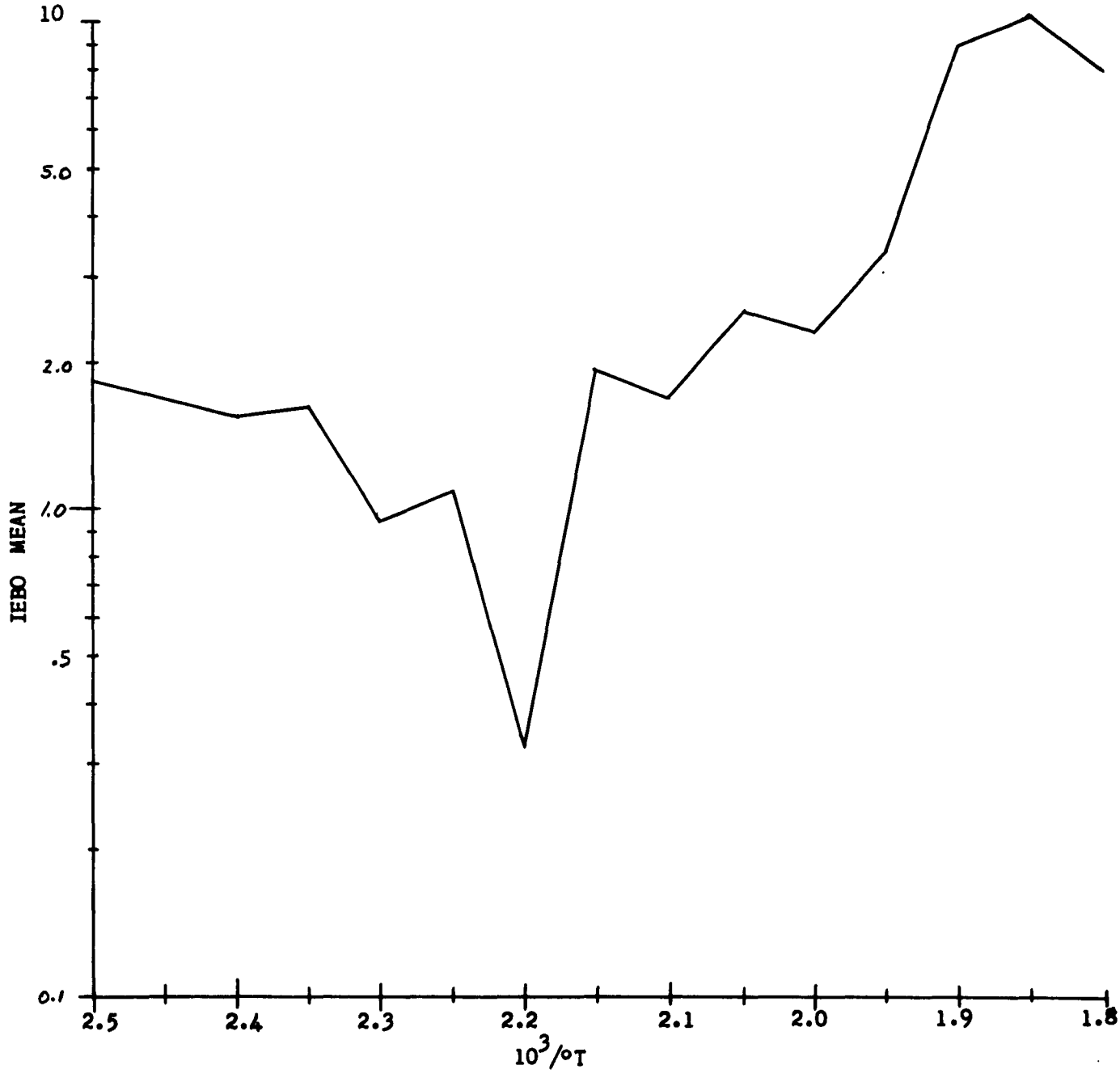


FIGURE 3.2.EE
LOG ICBO MEAN 3 HRS.

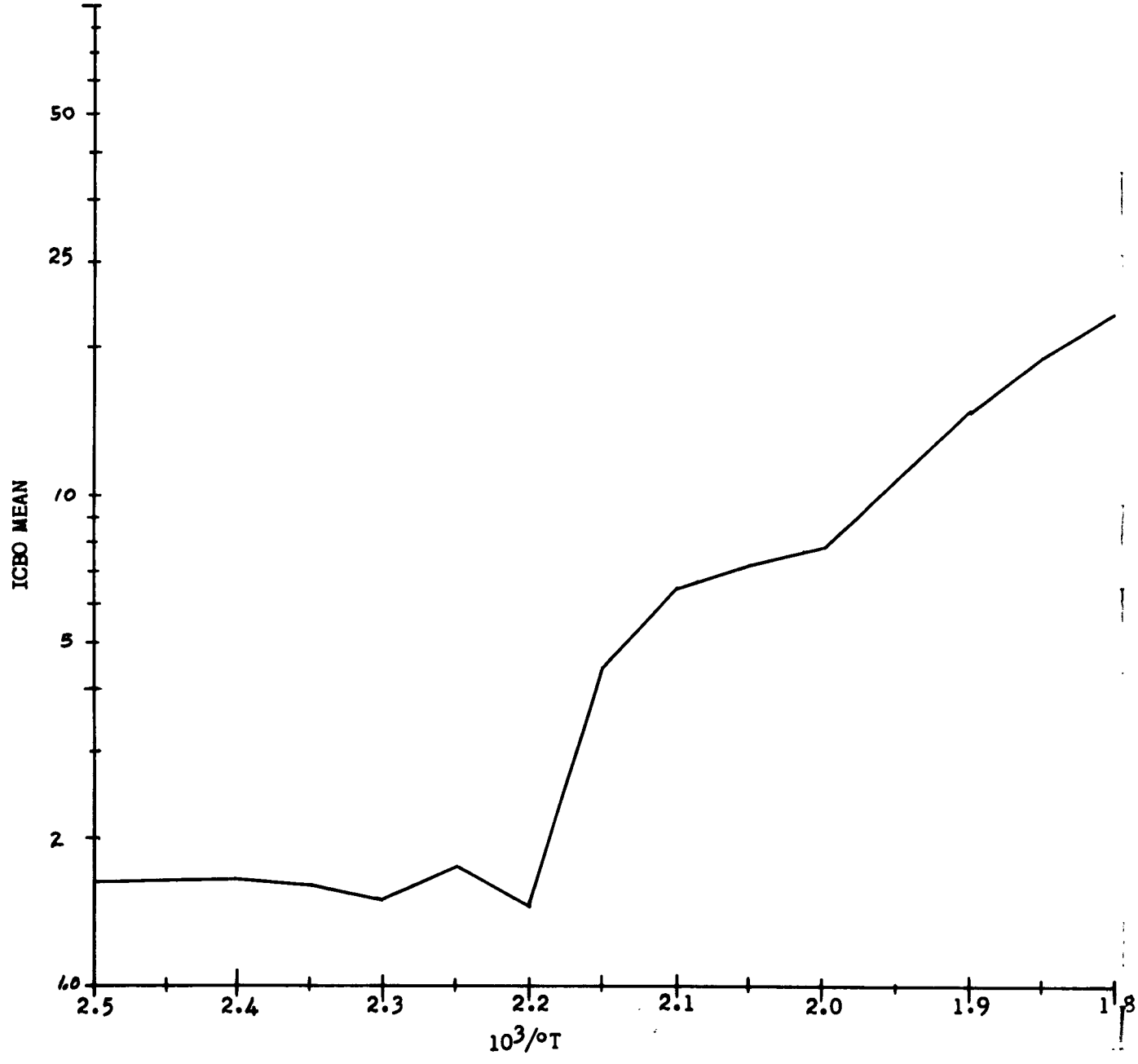
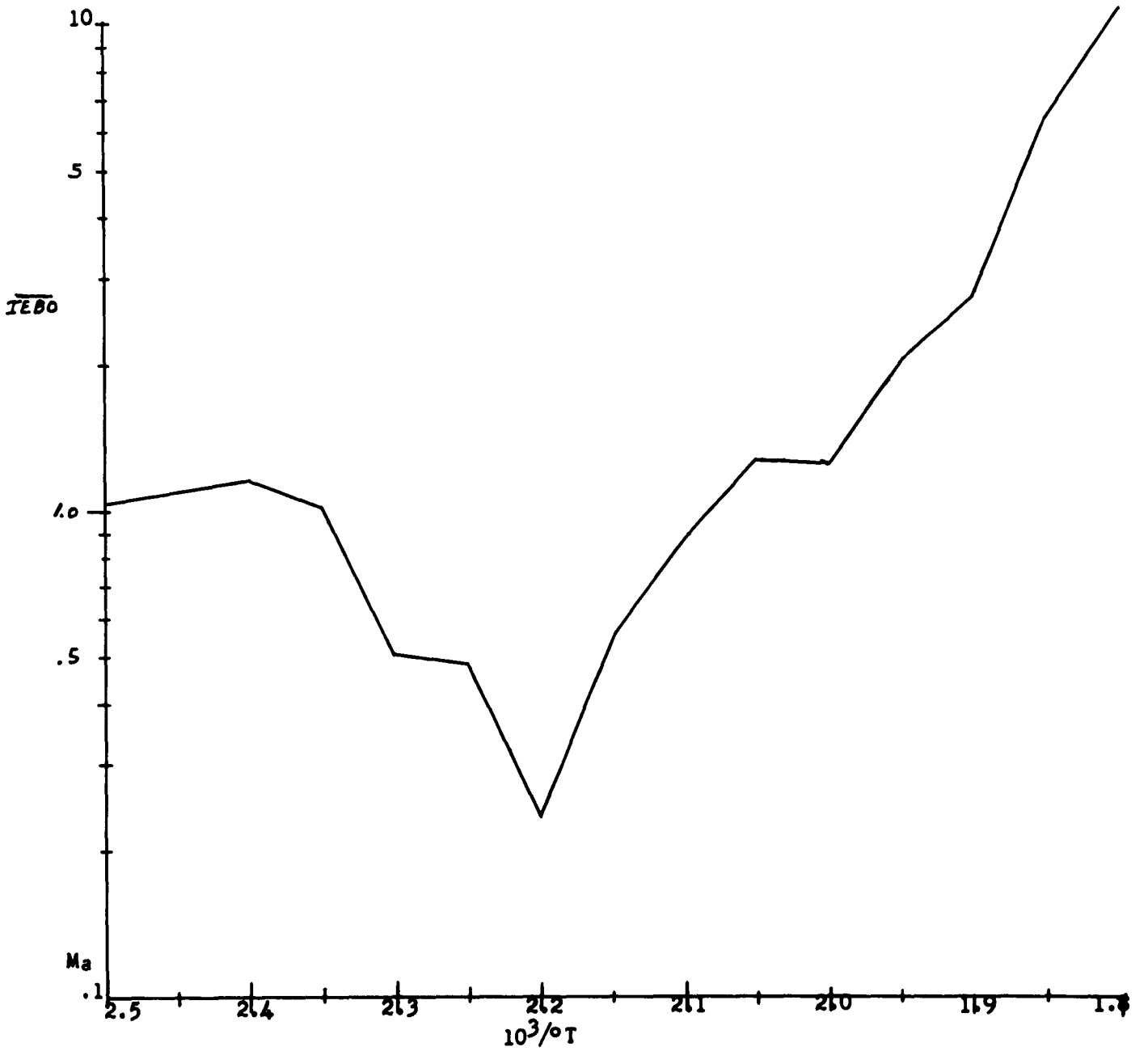


FIGURE 3.2.FF
LOG IEBO MEAN 3 HRS



Conclusions. The accelerated pulse test demonstrated the unique mode of failure anticipated - in substantial quantity. Initial step-stress experiments and analysis of same show promise as an early reliability detection method.

Program for the Next Quarter. The second pulse life sample will be tested and analyzed. The step-stress data presented above will be further investigated and further experiments conducted. The accelerated 158°C storage testing will be completed and analyzed.

3.3 FAILURE ANALYSIS PROGRAM - J. R. Bevington.

During the past quarter, the Failure Analysis Group has analyzed several hundred device failures from the 135°C storage life daily sampling program on raw production materials. The results of these analysis have been reported back to the Manufacturing, Engineering, Process, and Quality Control personnel through the weekly P. E. M. Meetings, as well as in several special written reports. A special analysis of failures from accelerated step-stress tests has also been performed to determine the degree of correlation of failure mechanisms with those found at normal stresses.

An analysis has also been made on all test failures from the Milestone I tests and the related pulse life test group. Special studies on specific failure mechanisms have been performed to gain more insight into various problem areas.

3.3.1 Facilities and Capabilities.

General and Engineering Status. X-ray radiographic techniques have been improved and several radiographic studies performed on large round power devices. No particles have been been detected in over 200 devices examined of the high reliability large round power type using X-ray radiographic techniques. Photo processing services are now available for X-ray developing in the R & E Building, which permits more efficient processing and closer liaison. Equipment for metallurgical grinding and polishing setup have been received and installed in the Failure Analysis Laboratory. This equipment is operational and cross-section techniques are now being optimized.

A direct reading, two axis, telemicroscope has been obtained for the Failure Analysis Laboratory. Scale divisions as low as .01mm are available. Possible applications of this instrument include micro measurements on X-ray negatives and application to micro-probe techniques.

Continued liaison has been maintained with the advanced analytical laboratory at the Delco Remy Division of G. M.

Conclusions. Laboratory capabilities have been increased through improvements in X-ray radiographic techniques, closer proximity of developing facilities, procurement and installation of metallurgical sectioning and polishing equipment, and the procurement of a telemicroscope.

Program for the Next Quarter.

1. Establish X-ray radiographic resolution capabilities in accordance with Mil-Std and ASTM procedures.
2. Complete optimization of cross-sectioning techniques.
3. Initial development of wet-chemical qualitative analyses techniques.

3.3.2 Failure Analysis - 135°C Daily Sampling Program.

General and Engineering Status. A continuing analysis of failures from the 135°C program has been made. All device

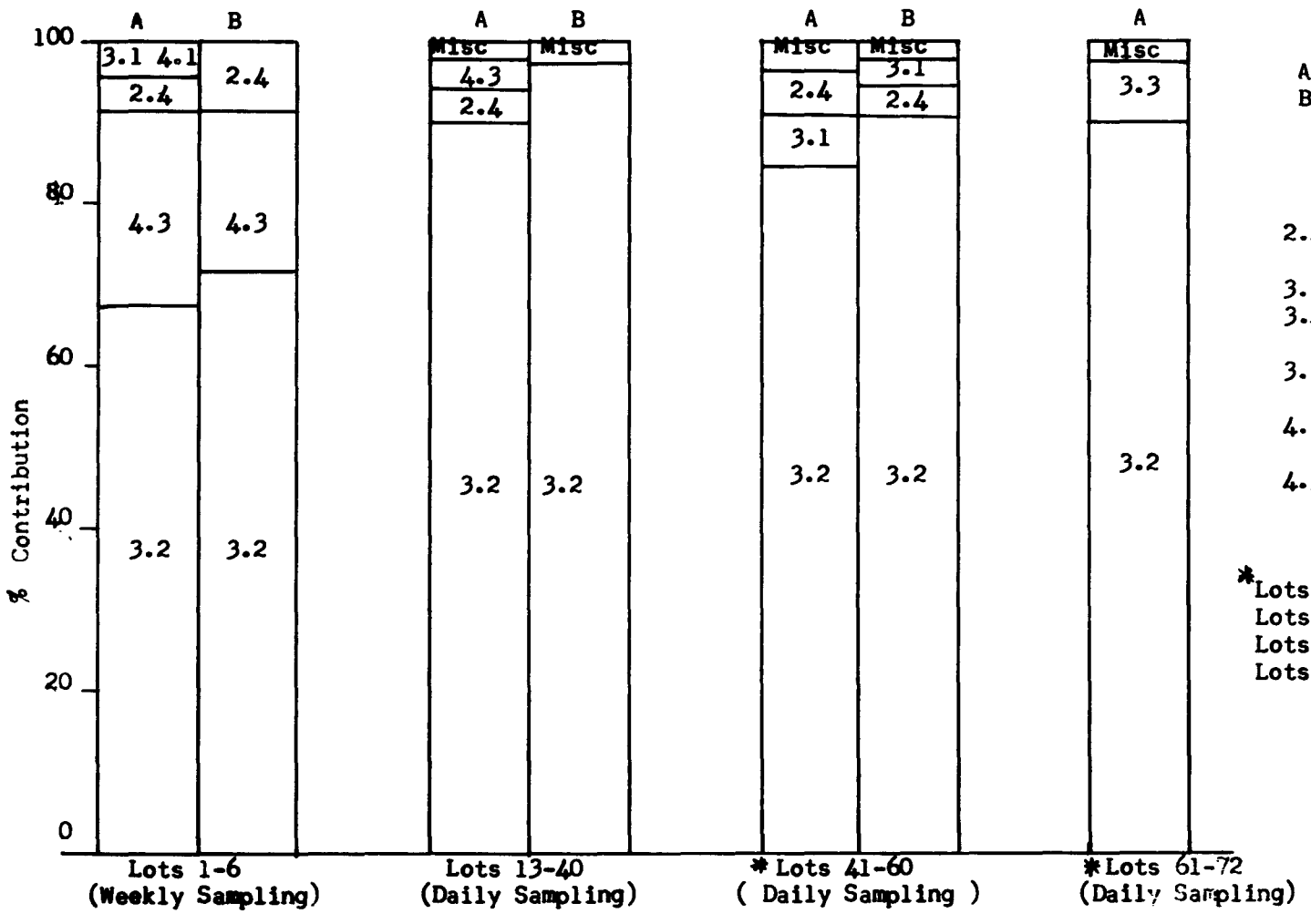
failures have been logged and failure modes assigned. A bar graph showing failure mode percent contribution by time periods is shown in Figure 3-3A.

The major mode of failure is collector diode degradation (Mode 3.2). This mechanism has been traced to surface conditions and the devices are recoverable after opening by various cleaning and outgassing techniques. For a detailed discussion on surface studies, refer to Section 3.4.

Aside from the major surface problem involving up to 90% of the 135°C failures, a unique condition was detected in the time period represented by Lots 41-60. Initial detection of this problem came from a submission of devices of a type similar to that in the PEM Program. These units had exhibited a slightly looped and sagging characteristic in the portion of the emitter and collector reverse diode curves before the knee. A microscopic examination of the crystal surfaces revealed a striated poly-chromatic film residue which seemed to emanate from the base ring solders. Attempts to remove this film with outgassing and surface cleaning techniques were unsuccessful. Samples of this material were then submitted to electron diffraction analysis and the film was identified as tin oxide. It is significant that one of the ingredients of the base ring solders and coatings is tin.

This condition was subsequently found in varying degress in failures from Lots 40 to 60 with a peak reached in Lot No. 47. Analysis of more recent materials does not reveal the presence of this condition and it is believed that this condition is under control.

Failure Mode Percent Contribution
135°C Storage Life
Sampling Program



Letter Code

A. 0-500 Hours
B. 501-1000 Hours

Number Code

2.4 Vebo degradation surface effect.
3.1 Gain degradation.
3.2 Vcbo degradation surface contamination.
3.3 Vebo degradation surface contamination.
4.1 Crystal fracture (Vertical)
4.3 Crystal fracture (Horizontal)

*Lots 41-50 complete to 1000 hours
Lots 51-63 complete to 500 hours
Lots 63-70 complete to 333 hours
Lots 71-72 complete to 167 hours

Fig. 3-3-A

In Figure 3-3-A, an increase in percent contribution for Mode 3.1 (low gain) is noted in Lots 41-60. These failures were traced to excessive base width conditions and were in the low gain portion of the distribution initially. The occurrence of this condition appeared to be random as there was no observable increase in base width on other devices from the same lots. The lots which exhibited this condition covered the same time period during which the tin-oxide film was noted, although a relationship has not been established. Recent materials have not exhibited this condition.

Mode 2.4 (emitter diode degradation due to surface defects) shows an increase in percent contribution during Lots 41-60. Almost all of this contribution came from two lots (No. 53 and No. 58) and resulted from excessive emitter solder shrinkage and wisp formation on that material. There have been only insignificant contributions to failure on later lots. For a more complete discussion of investigations of this mechanism, refer to Section 3.1.20.

The occurrence of Mode 4.3 related to peripheral spur regrowth which made a significant contribution in the earlier analyses, has dropped to less than a 2% contribution. The conditions which tend to generate this mechanism have been improved; however, as a latent mechanism is involved, a detailed investigation and study program is continuing. The details of these efforts may be found in Section 3.1.18.

Conclusions. The major percent contribution to failure continues to be Mode 3.2. An increase in Mode 3.1 contribution was traced to a random occurrence of excess base width and an increase in Mode 2.4 contribution was traced to two lots which

exhibited excessive emitter solder shrinkage and wisp generation. A further reduction in the Mode 4. 3 contribution reflects the efforts of a major improvement program on spur regrowth reduction.

Program for the Next Quarter.

1. Analysis of failures from the 135°C storage sampling program will continue to provide informational feedback to the Manufacturing, Process, Engineering, and Q. C. Groups.

2. Specific investigations of mechanisms involving Modes 3. 2, 2. 4, and 4. 3, are being conducted by specially assigned groups. The failure analysis efforts in these areas will be to assist the assigned groups as required and to monitor improvements.

3. 3. 3 Failure Analysis - Step-Stress Failures.

General and Engineering Status. A complete analyses of step-stress failures has been made to determine if the failures generated represent the same mechanisms observed in lower level constant stress tests. The results of the analyses of temperature step-stress tests revealed that the same mechanisms of failure are present as those found on elevated temperature storage. The mechanism involved is diode degradation resulting from surface conditions. These failures recovered identically with those generated in storage life tests and the failure indicators were identical.

Conclusions. The failures generated in temperature step-stress testing appear to be identical to those found in elevated temperature storage life testing. The results indicate that this test satisfactorily accelerates mechanisms present at lower constant level temperature stresses.

Program for the Next Quarter.

1. Analysis will be performed on all step-stress failures generated in the step-stress study program being performed by the reliability group. Attempts will be made to identify the mechanisms of failure present and to compare them with the comparable lower level constant stress test failures.

3.3.4 Failure Analyses - Milestone No. 1.

General and Engineering Status. An analyses of the 14 failures from the 135°C storage portion of the Milestone I test indicated that the mode of failure was collector diode degradation resulting from surface mechanisms (Mode 3.2). The failure indicators and the results of the recovery techniques used indicate that this is the same mechanism as that observed in the 135°C daily sampling program.

A unique late incidence of failures on this material and in that of comparable Lot No. 44 (daily sampling program) may possibly be related to a tin-oxide residue problem identified during that period of manufacture (see discussion in Section 3.3.2).

Eleven of thirteen operating life failures were attributed to Mode 2.6 (collector to base shorting). In most cases, this shorting was accompanied by a solder protuberance from the base ring solders. These failures were related to emitter micro-wisps in several instances, and to collector diode anomolies on several other devices. These units were documented 100% by curve trace analyses prior to test. In almost all instances, initial pre-failure indicators were found in the diode trace characteristics. The study of dynamic trace pre-failure indicators is a continuing program in the Failure Analysis Group and further studies are planned. Of the two remaining devices, one failed by a collector to emitter short with the actual mechanism not established; the second unit was not defective. It was found that a small solder ball on the test tray had resulted in a short indication during test out.

All 28 pulse life test failures involved a mechanisms involving an outward creepage of the emitter solders. All but one had shorted collector to emitter through a breakdown mechanisms. The other device had a low resistance short between emitter and base caused by the creepage of solder across the junction which did not result in breakdown to the collector. The mechanism involved at this 600 watt-60°C pulse stress is not the same as those observed at lower stress pulse testing. The validity of failure rates on this test is therefore reduced. It is felt that a threshold power dissipation-temperature ambient level has been passed which allows the solders to become molten or plastic and results in solder movement. This condition has not been observed on failures from pulsed power applications. As the high current level (10A) results in high current levels in the outer emitter periphery and the high pulse power dissipation

Fig. 3-3-B

Fig. 3-3-C

Typical Mode 2.1 Pulse Life Failure:

Solder creepage across junction with subsequent violent breakdown to collector. Solder protuberances are from the emitter indium. (Found only at 600 W-60°C pulse levels)

Fig. 3-3-D

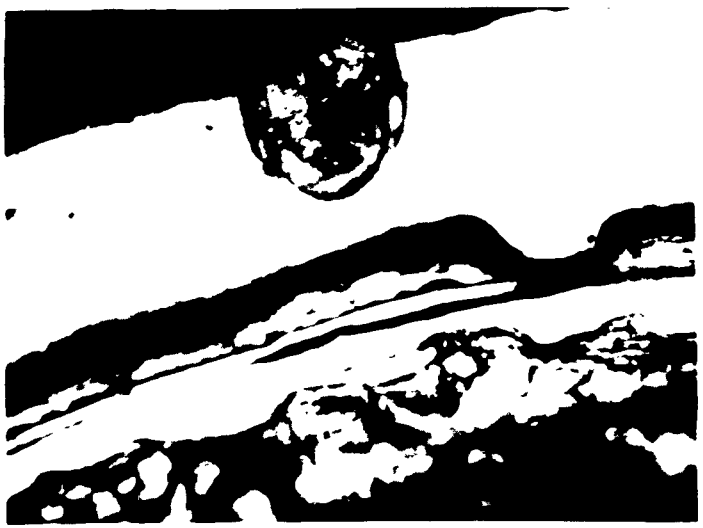


Fig. 3-3-E

Typical Mode 2.6 Operating Life Failures

Breakdown collector to base followed by a protuberance development from base ring solders.

(600W) and temperature ambient (60°C) results in higher internal operating temperatures; this test might indicate devices which had conditions resulting in non-symmetrical current distribution, but this has not been verified.

It has been recommended that consideration be given to testing at a lower pulse stress level to achieve better correlation with failures found on normal pulse applications.

Following is a summary listing of failure modes assigned to Milestone No. 1 failures:

Test Stress	Mode 3.2	Mode 2.6	Mode 2.1	Mode 2.4	Good Device
135°C storage life	14	-	-	-	-
40V-90°C operating life	-	11	1	-	1
60V-10A-60°C pulse life	-	-	27	1	-

Conclusions. Milestone No. 1 failures in 135°C storage were related to surface conditions resulting in collector diode degradation. Operating life failures were due to collector to base shorts which were related to emitter micro-wisps and to collector diode anomolies. The mechanism of failure on the accelerated pulse life test involved a solder creepage conditions not observed at normal stresses. It is believed that a threshold level has been exceeded which results in the generation of a new mechanism.

Program for the Next Quarter.

1. Failure analyses will be performed on all Milestone test failures generated during the 3rd quarter.

2. Further studies of pre-failure indicators will be made on Milestone No. 2 material.

3.4 ANALYTICAL - EMPIRICAL SURFACE STUDY PROGRAM.

3.4.1 Surface State Analysis - M. E. Stanton.

A. Field Effect Measurements.

General. The analysis procedure for the field effect measurements has been established. An in-plant documentation has been made for future reference. This analysis will be used to determine the physical properties of the surface which are established by surface treatment.

Engineering Status. The apparatus shown in Figures 3-4-A and 3-4-B is operational. A gas train has been constructed which will allow ambient cycling from dry oxygen through wet nitrogen. The sample material with high bulk lifetime has been prepared. The bulk lifetime measurements show a lifetime of approximately 145μsec. The sample material has been sawed and lapped to $\approx$.010 inches. An impact grinding tool has been made to shape the sample. Samples have been shaped using this tool and leads have been attached. A three terminal capacitance measuring bridge has been constructed to determine capacitance between the field plate and the sample. Preliminary measurements have been made to check out the entire apparatus.

Program for the Next Quarter. During the next quarter, experiments will be conducted to determine the effects of surface treatments (Paragraphs 3.4.6 and 3.4.7) on the physical parameters. The first experiment will be with the chemical oxidizing treatment and the second with the boiling alcholol treatments.

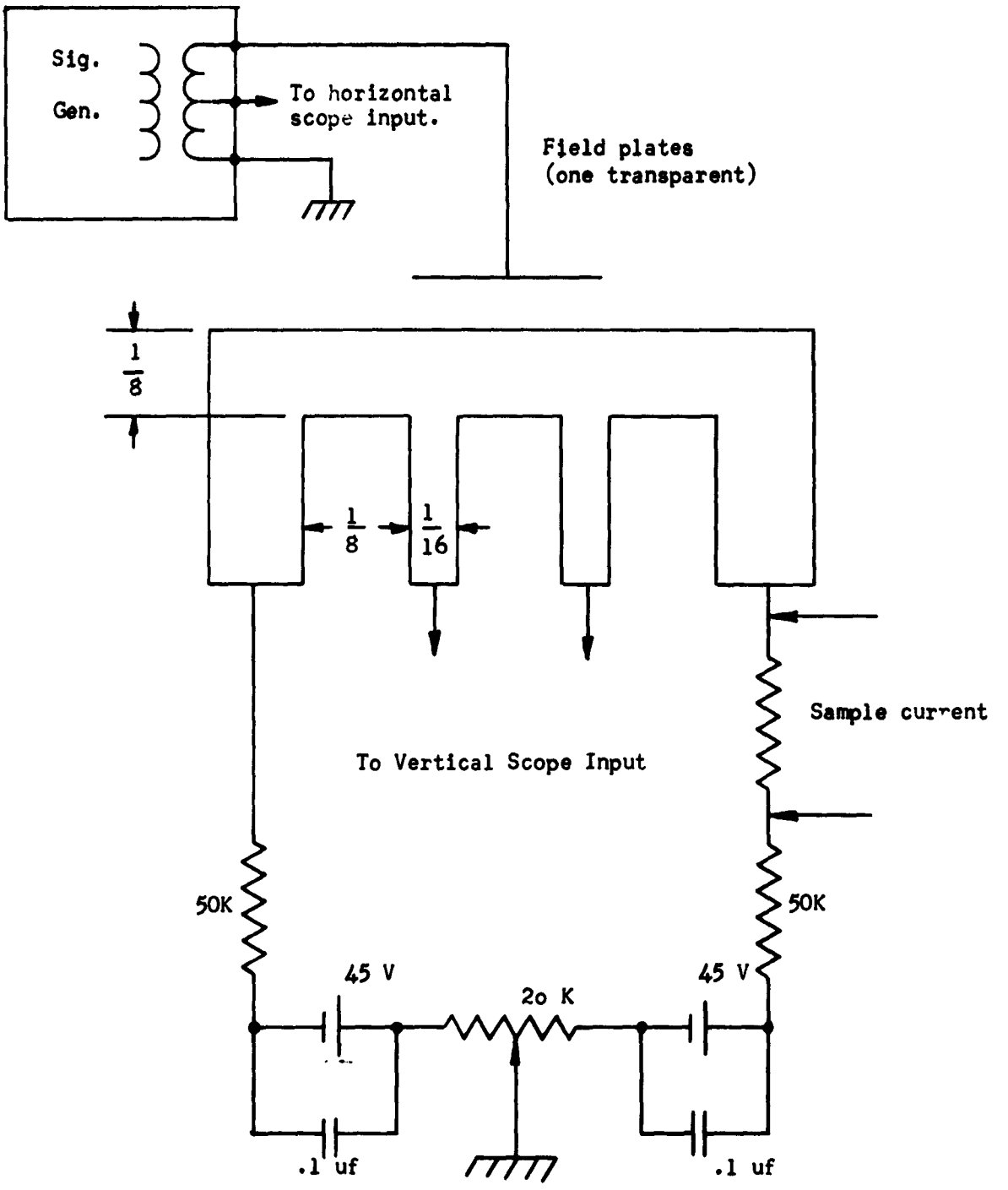


Fig. 3-4-A

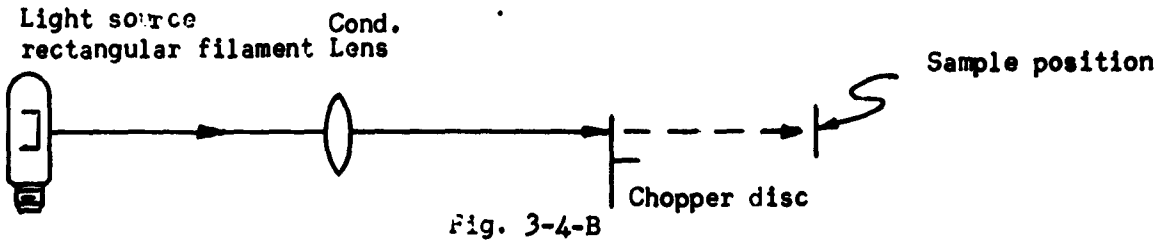


Fig. 3-4-B

Field effect measurements may be made to supplement the study mentioned in Section 3.4.1B.

B. Time Variation of Excess Collector Current.

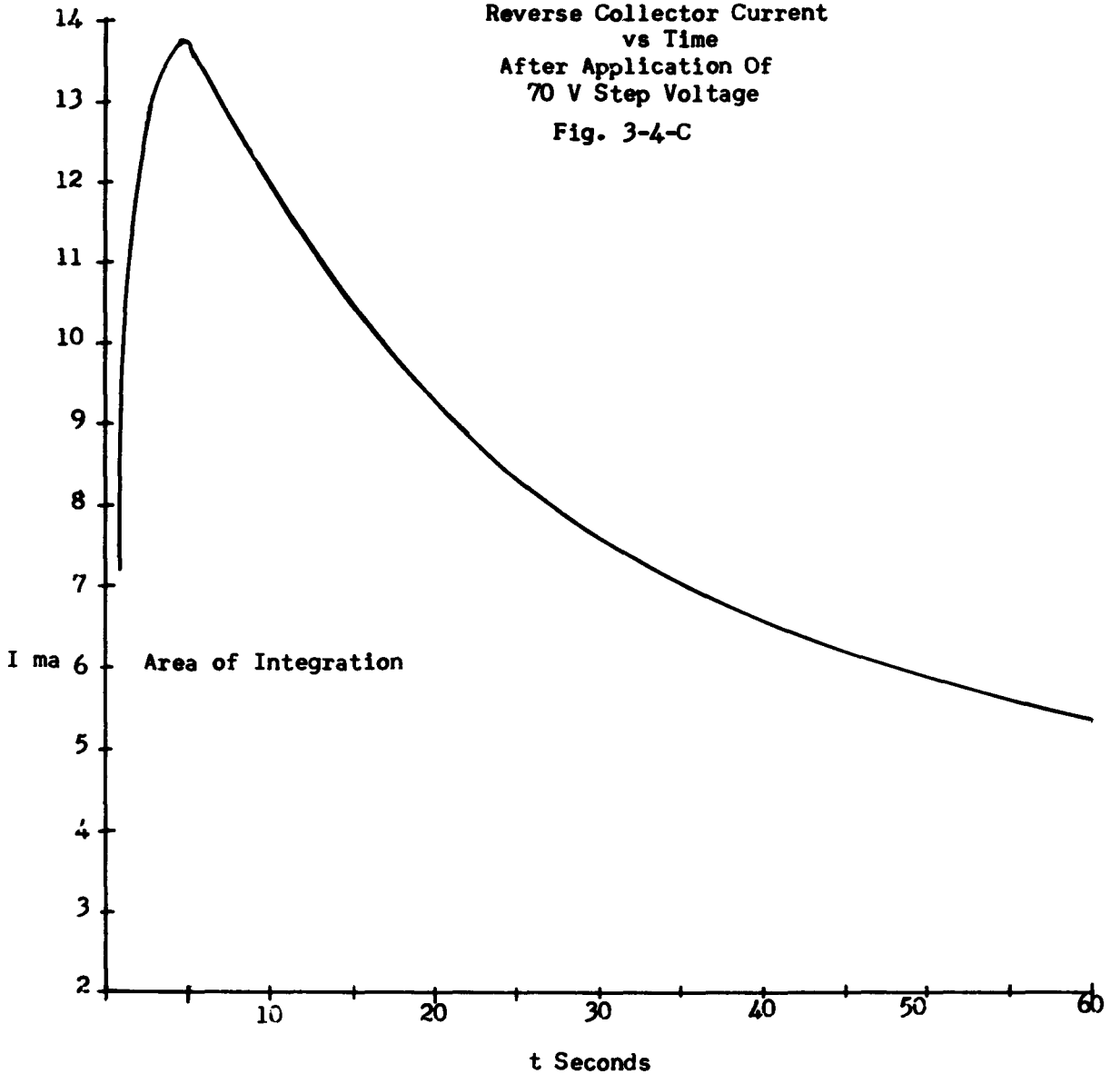
General and Engineering Status. A series of experiments on the variation of excess collector current in the 10 to 80 volt region has been run. This has been done in an attempt to describe, by a suitable physical model, this excess current. In these experiments, the diode was subjected to a step voltage reverse bias and the current variation with time was monitored. Three devices were studies. Device No. 1 was one which had failed (3.2 mode) in the 135°C storage program; device No. 2 was one which had successfully passed the 135°C storage stress; and device No. 3 was one which contained barium oxide as a desiccant.

A graph of ICBO with a 70V step is shown in Figure 3-4-C. It is noted that the current peak is not instantaneous as would be expected with a shunting path which is established on the unit at time = 0. The decay curve resembles an RC type decay and this was verified in Figure 3-4-D, which is a plot of log ICBO versus t for 3 values of the step voltage. The decay curves of Figure 3-4-D can be fitted with two straight line portions, the slope of which can be interpreted as decay constants ν_1 (nu) and ν_2. These constants are not voltage dependent. The rise time, however, is seen to be voltage dependent.

The time constants suggest a charge transfer to outer states. However, an integration of the excess current portion yields a total charge transfer much greater than can be explained by the number of states commonly associated with the outer surface.

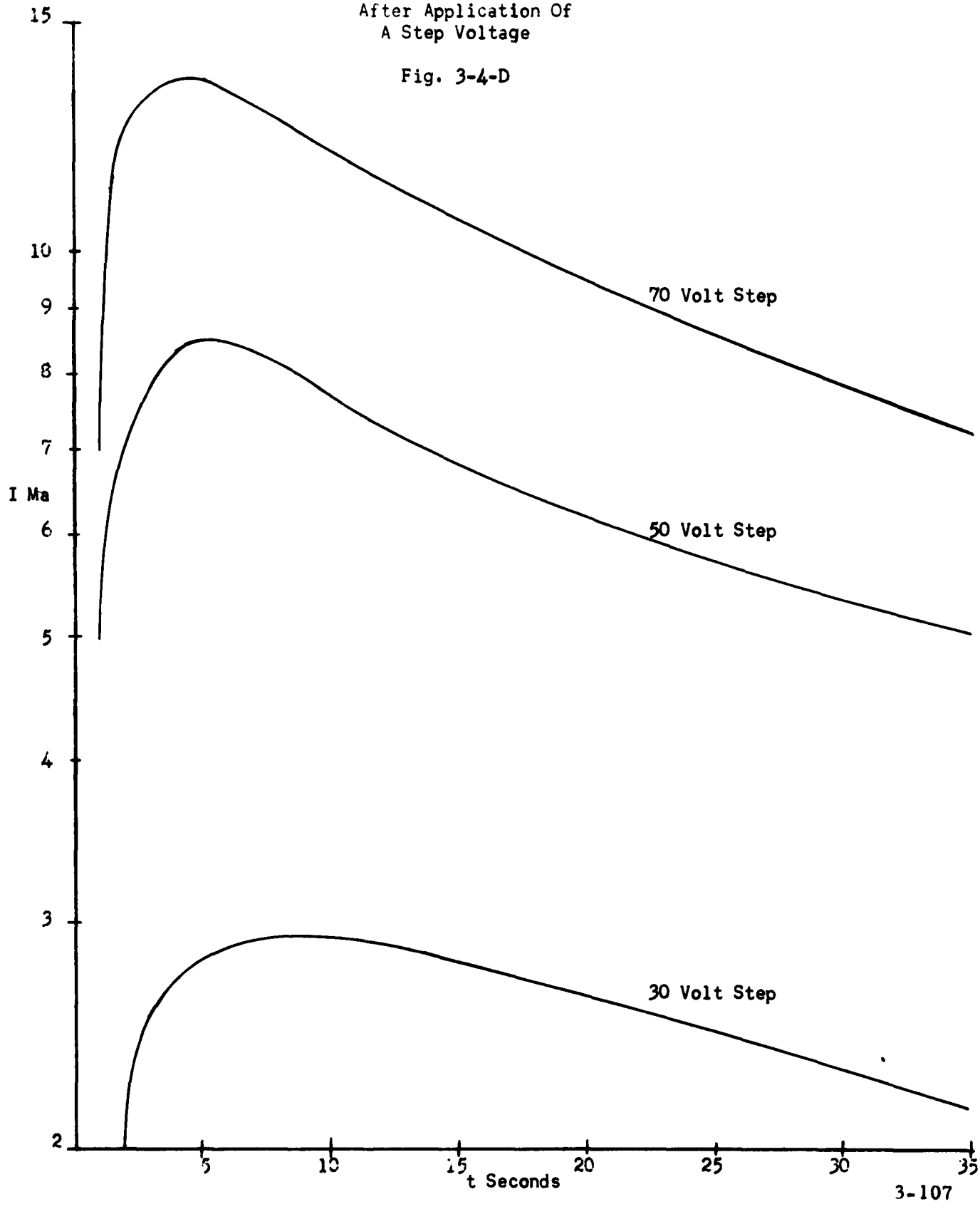
Reverse Collector Current
vs Time
After Application Of
70 V Step Voltage

Fig. 3-4-C



Excess Diode Current
vs Time
After Application Of
A Step Voltage

Fig. 3-4-D



The peak current and the current as $t \rightarrow \infty$ were plotted as is shown in Figures 3-4-E and 3-4-F. This indicates that the excess current could be ascribed to a time varying resistive path.

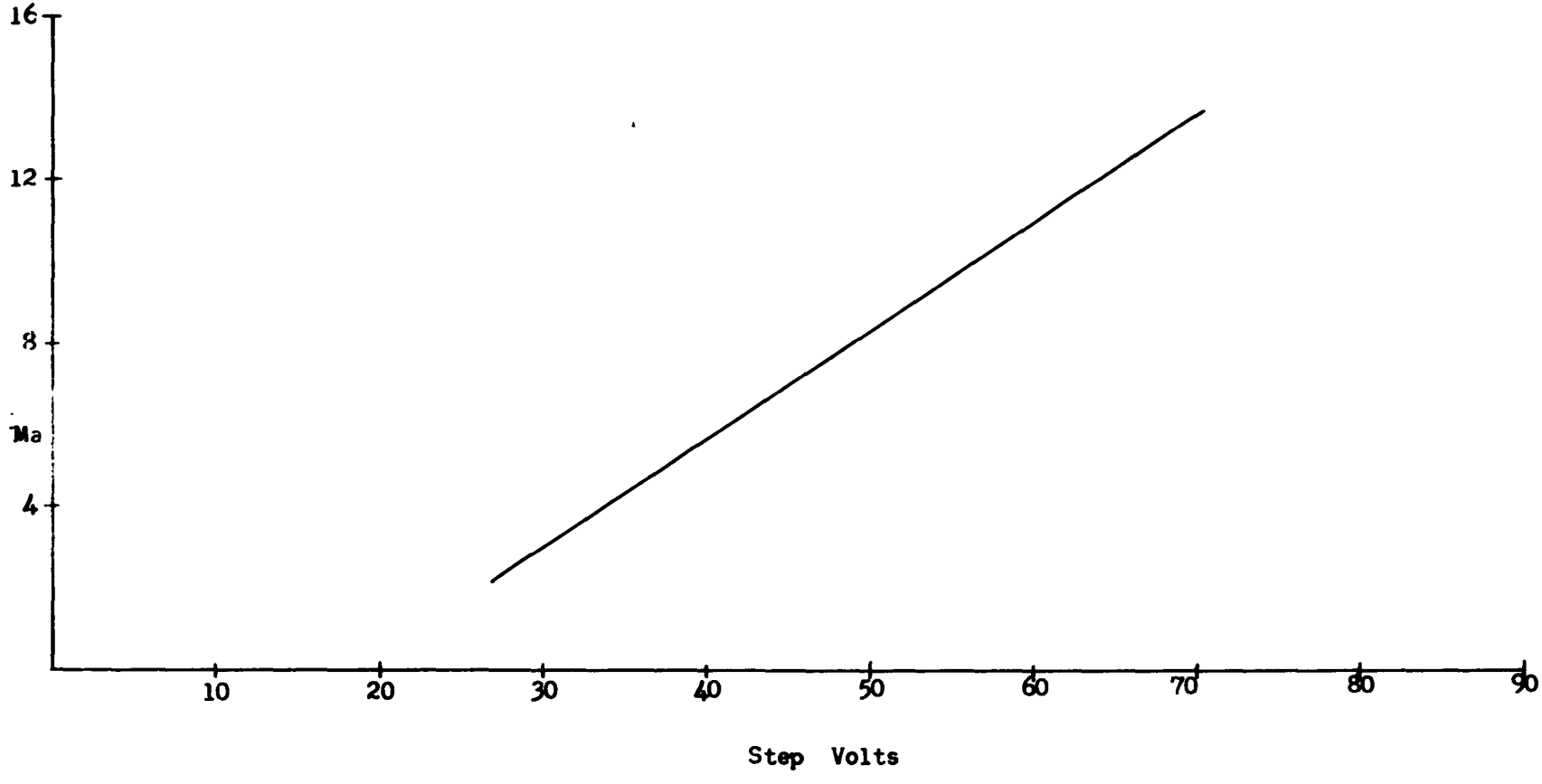
A similar study on unit 2 showed a lower peak current, but the same time varying relationships. Unit 3 did not exhibit the time varying relationship. Ba O lowers the vapor pressure of water by chemical reaction. Since it would not be expected to modify other portions of the ambient, which have been shown by residual gas analysis, it may be concluded that the time varying characteristic may be associated with H_20. Conclusions can not be drawn about the quantitiative part of H_20 in the time varying characteristics. In other words, water may be a necessary condition for the phenomena, but not a sufficient condition.

A unit which has been washed in de-ionized water and alcohol does not exhibit the time varying characteristic, even when exposed to H_20 vapor. The same unit, however, does exhibit the time varying relationship when exposed to vapor above NH_4OH. Whether this result could be obtained with other vapor has not been determined. The creeping of diode breakdown as the voltage is slowly increased and the hysteresis loop in the diode curve often associated with unreliable units is shown in Figure 3-4-G.

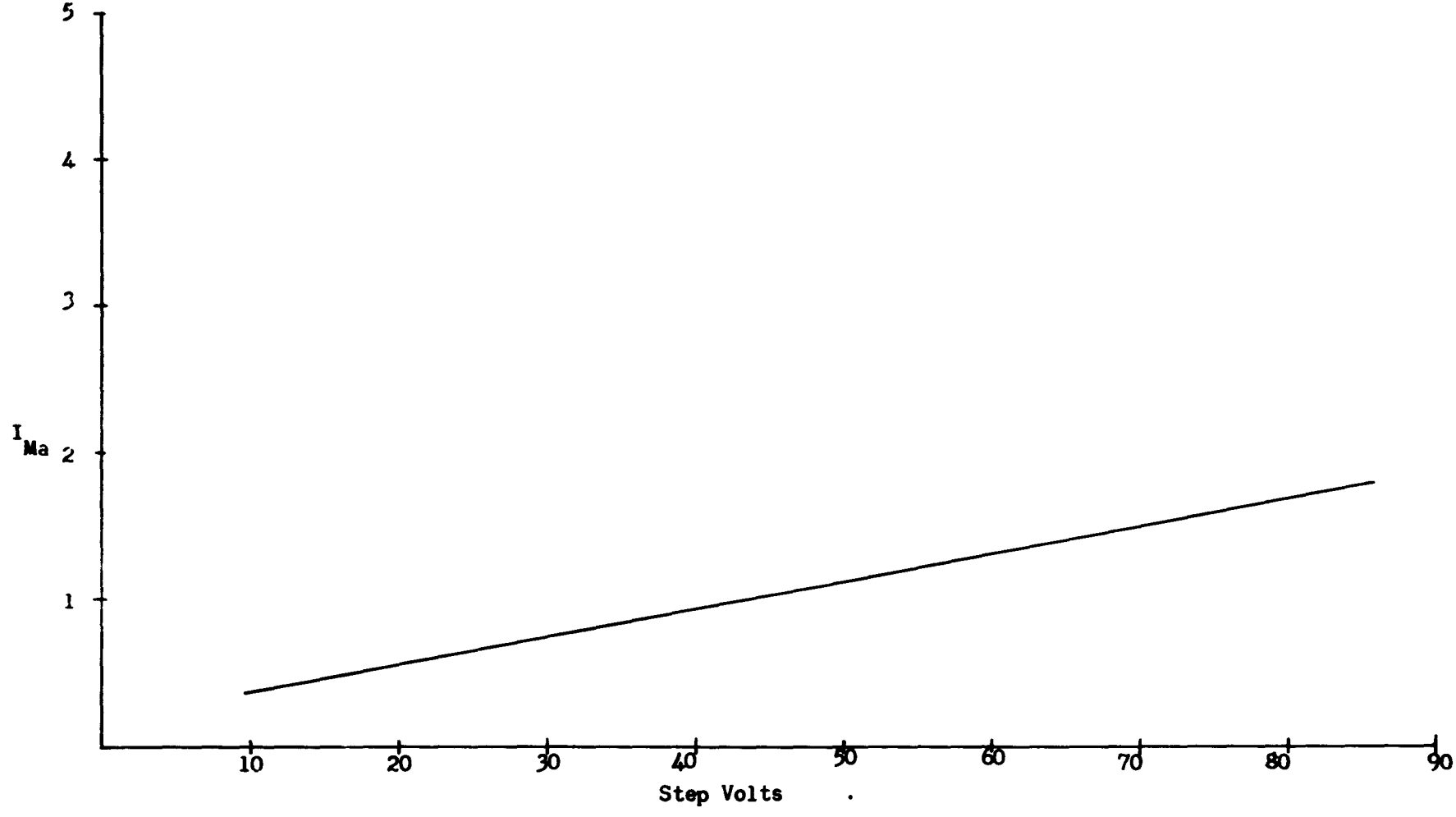
The looping effect can be readily deduced by noting the difference between the rise and the delay times. The creeping effect as the voltage is slowly increased during dynamic sweep can be qualitatively deduced in the following manner:

Peak Collector
Current.After
Application of Step Voltage

Fig. 3-4-E



Collector Current Time ($t \rightarrow \infty$)
After Application of Step Voltage
Fig. 3-4-F



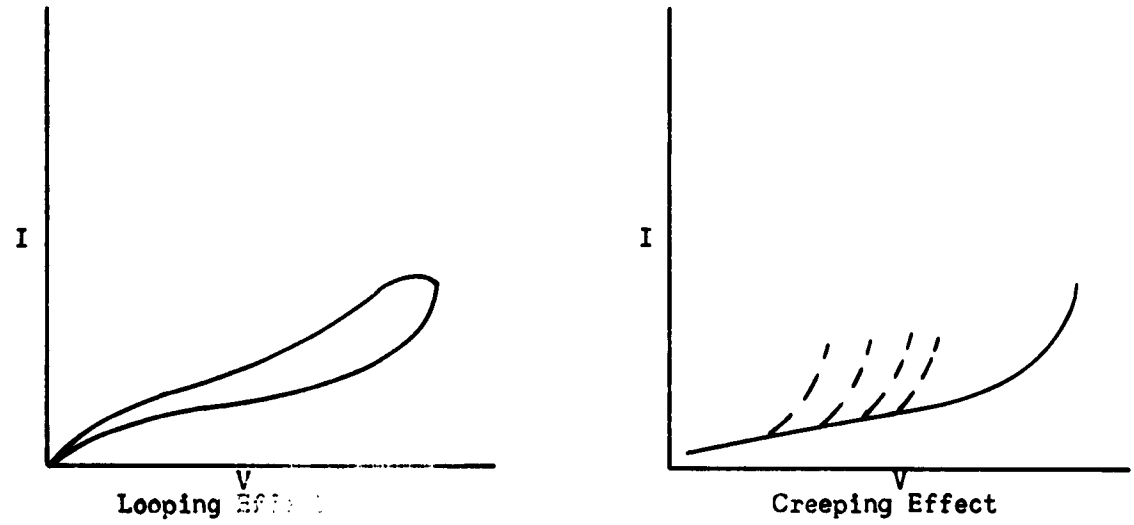


Fig. 3-4-G

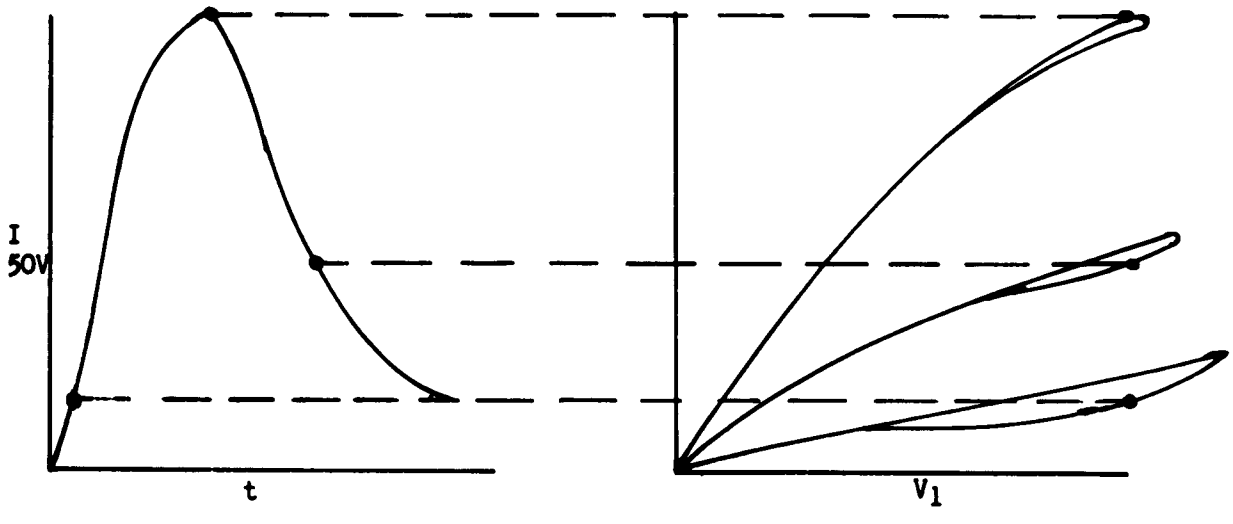


Fig. 3-4-H

The dynamic sweep goes through a current maximum similar to the step voltage case as shown by a time exposure of the dynamic curve trace after the instantaneous application of a 50V peak full wave sweep. This is shown in Figure 3-4-H.

Now as voltage is incrementally increased during dynamic sweep, the current can be considered as following a superimposed set of current curves as shown in Figure 3-4-I.

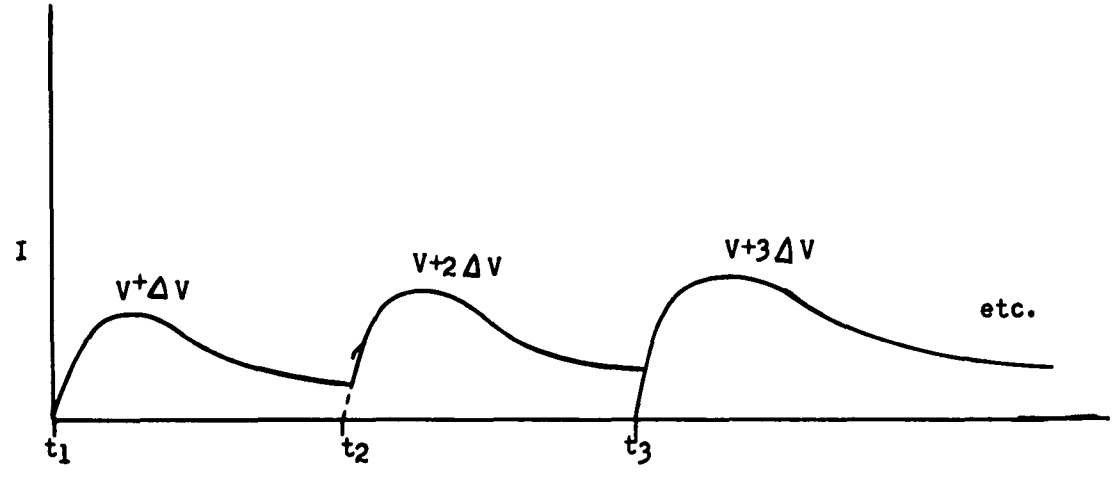
It has been noted that a polar solution rinse yields a similar looping effect on the dynamic curve trace. Since water is a polar substance, it is possible that the polar property of the adsorbed water layer on the germanium surface is involved in the excess collector current phenomena.

There are two considerations of the time varying characteristic when testing the device. The first, and most obvious from Figure 3-4-C, is that the wide current variation of the collector diode is found to occur in a time which is of the same order as the normal testing time of the device. It is important then that measurements which are used to compare the product be made after a well specified time after application of the reverse bias. Since the rise time is affected by the past voltage history (up to several minutes) of the diode, sequential testing will also alter the results.

The second application of the time varying phenomena to a testing program is in modulation life testing. With fixed amplitude sinusoidal modulation, ICBO would be expected to go through the current maximum at the start of the test and return to an equilibrium value for the remainder of the test. However, if the amplitude is allowed to vary with time, or the modulation frequency is

Qualititative Description of Creeping Effect

Fig. 3-4-I



randomly varied so as to exceed the frequency response of the device for appreciable time periods, the collector voltage may simulate the incremental voltage situation shown in Figure 3-4-H. If this occurs while the average dissipation of the device is high, the excess dissipation due to change in collector impedance may over-dissipate the device and result in punch-through, which is typical of modulation life failures.

Program for the Next Quarter. The effect of other polar molecules on the surface of the device will be made using the same experimental procedure.

Some possible implications of this time varying characteristics on reliability testing have been pointed out. The correlation of such results constitutes a major study in itself, and at present, there is no such program outlined.

A physical model of the excess current phenomena is suggested. This model is that the oxide + H_2O layer be treated as a semiconductor with the Fermi level placement dependent upon charge population in trapping levels; namely, the slow states commonly associated with the outer surface. The time constants which are observed are similar to those described by Morrison [1] and Kikuchi [2], and ascribed to charge transfer to slow states. The linear dependence of time constants of voltage were also observed by Kikuchi. The semiconductor model of the oxide layer will then account for the apparent gain in the observed charge transfer mechanism. Other models may describe the observed results and for that reason, further analysis of physical models will be made in the next quarter.

[1] S. Roy Morrison, Semiconductor Surface Physics, University of Penn. Press, 1956.

[2] M. Kikuchi, J. Phys, Soc., Japan, 9, 130 (1954); 9, 655 (1954).

C. Two Volt Diode Current Versus Temperature.

General and Engineering Status. The 2 volt diode current was monitored as the temperature of the device was varied through a cycle from room temperature to dry ice temperature, and back to room temperature. The measurement is used to determine a "dew point" by noting an increase in the diode current as the conducting path on the surface goes through a phase change.

An experiment was conducted on three units which did not fail on the 135°C storage program, and six units which did fail (3.2 mode). These curves are shown in Figures 3-4-J through 3-4-R. No current increase is noted in the three good units and the current increase was noted on five out of six of the failed units. The noted current increase occurs in some cases as it is warmed. This, at present, is not explained, but it is possible that the time of the cooling cycle needs to be controlled.

A larger sampling was attempted in the 135°C storage program but no correlation was established between potential failures and "dew point" indications.

Program for the Next Quarter. Another attempt will be made to correlate the dew point measurement with diode degradation. Careful attention will be given to the cooling cycle used.

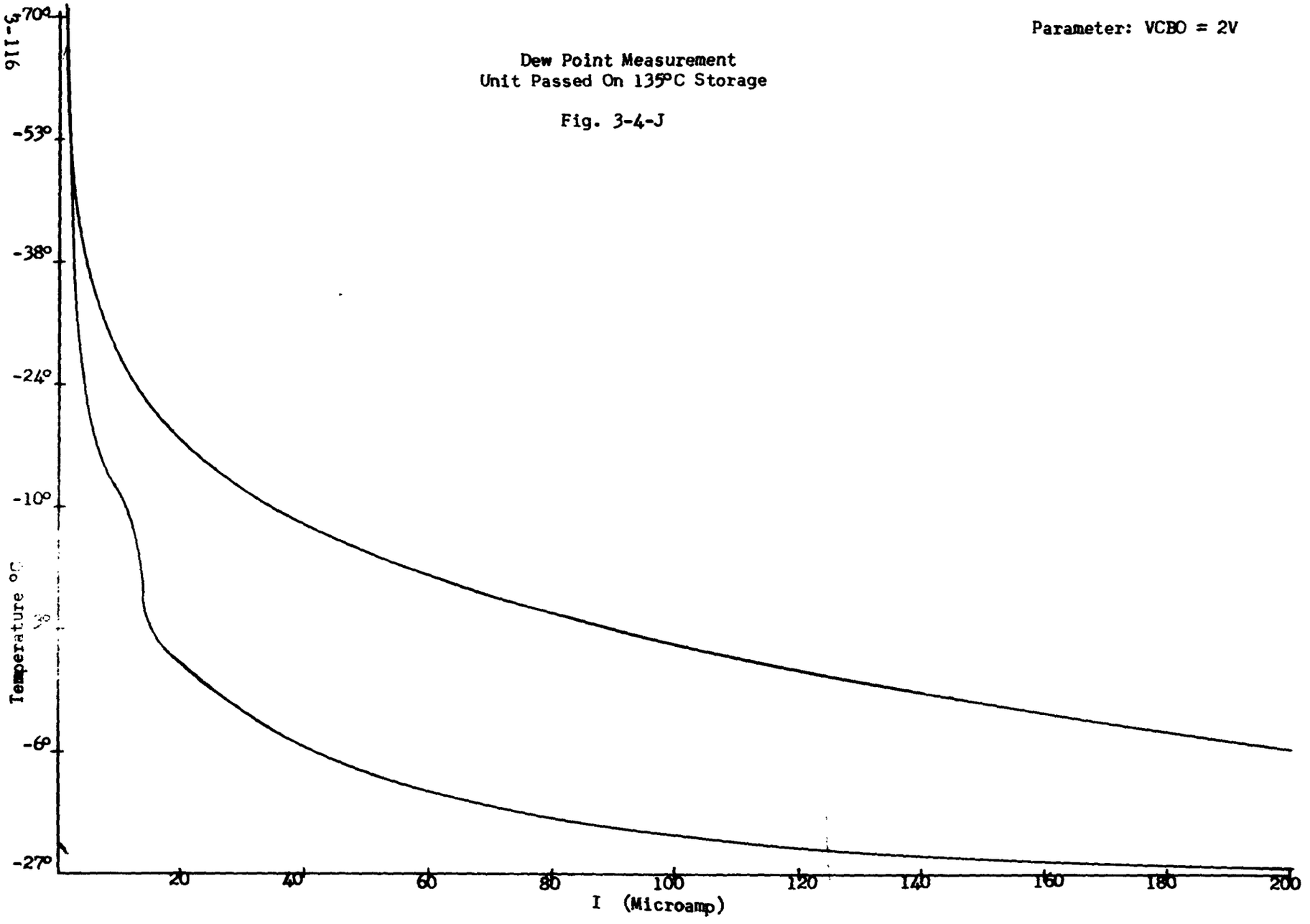
3.4.2 Residual Gas Analyzer - M. E. Stanton.

General and Engineering Status. The residual gas analyzer has been modified to permit reversible experiments and calibration

Parameter: VCBO = 2V

Dew Point Measurement
Unit Passed On 135°C Storage

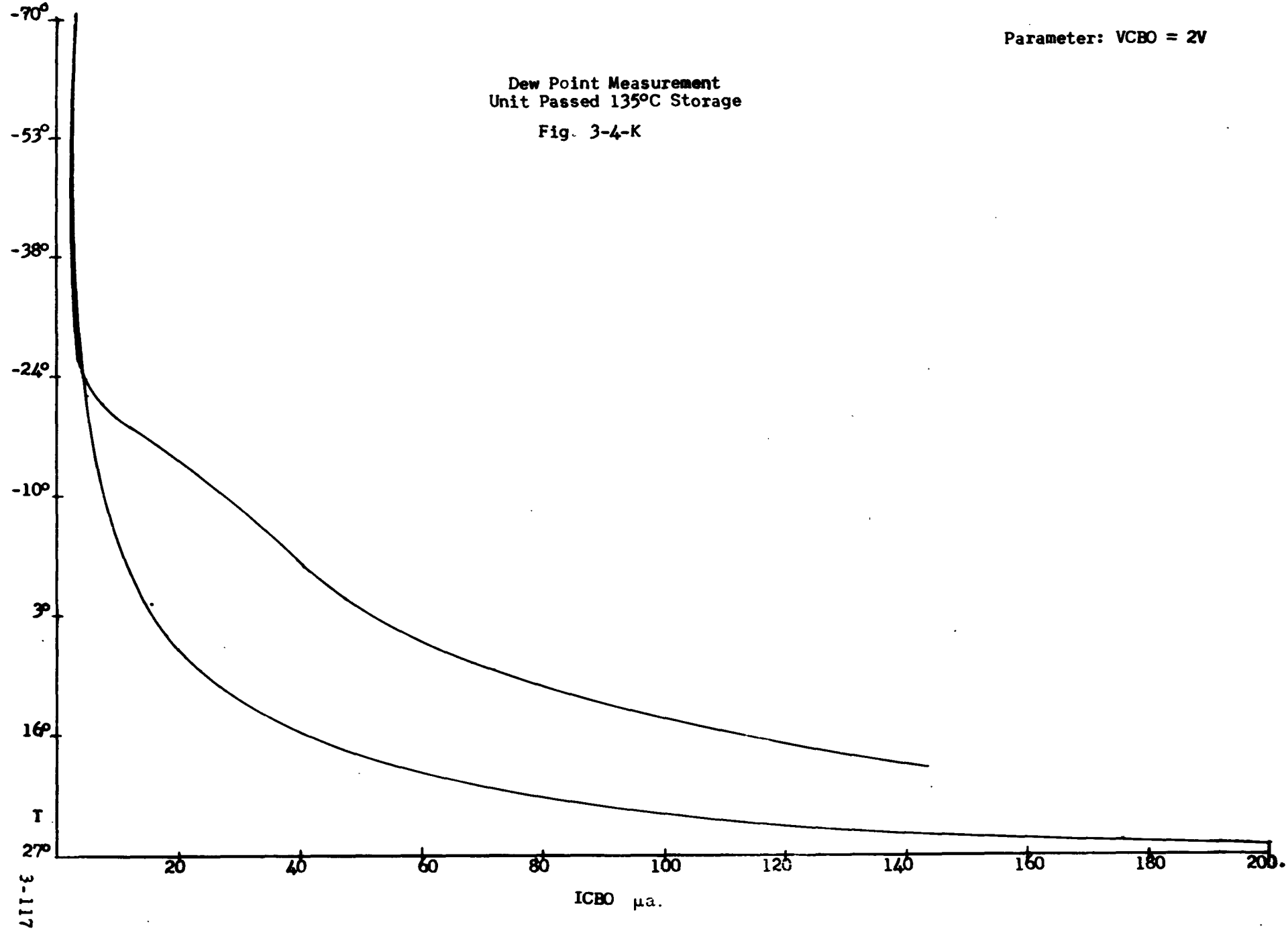
Fig. 3-4-J



Parameter: VCBO = 2V

Dew Point Measurement
Unit Passed 135°C Storage

Fig. 3-4-K



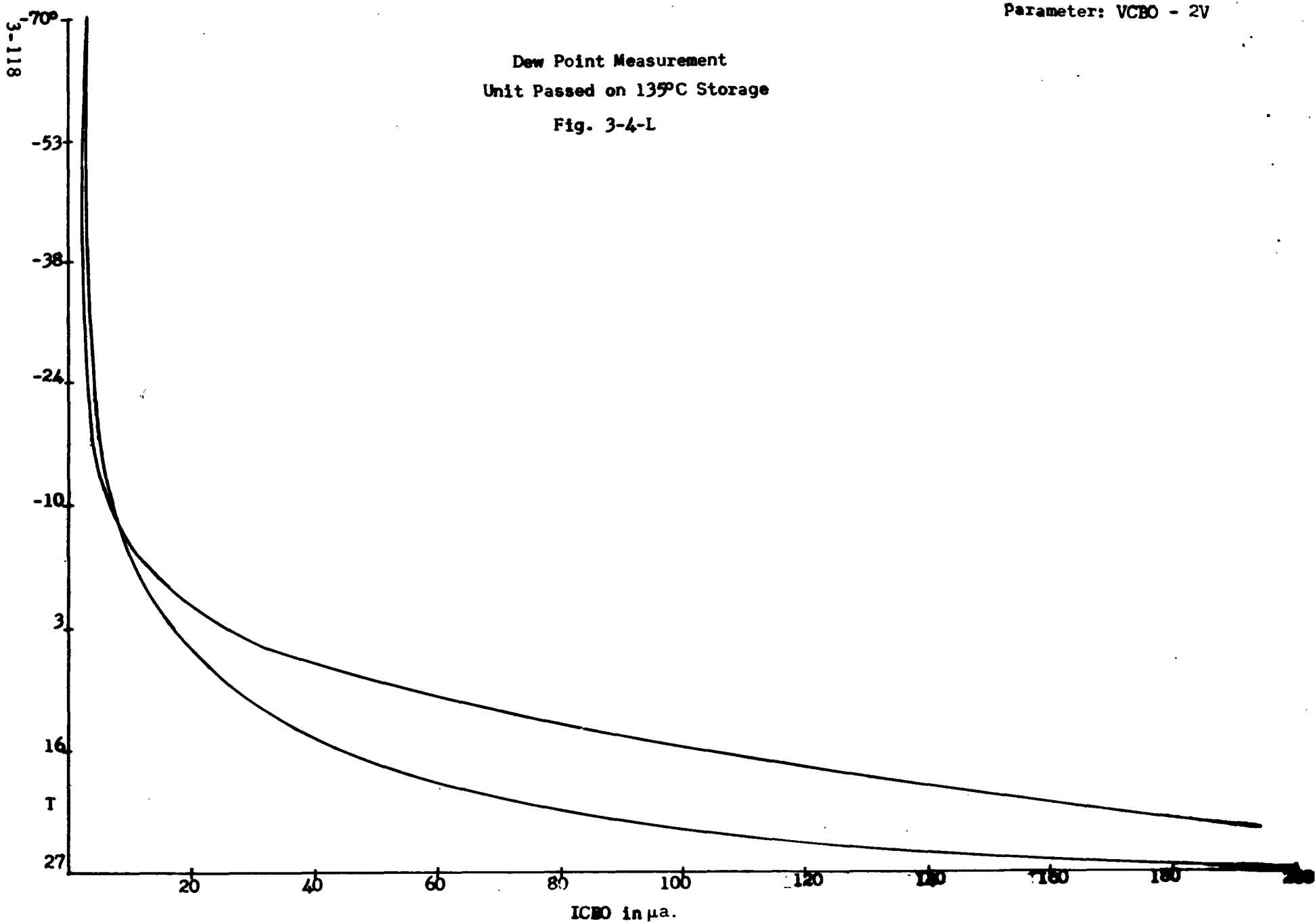
Parameter: VCBO - 2V

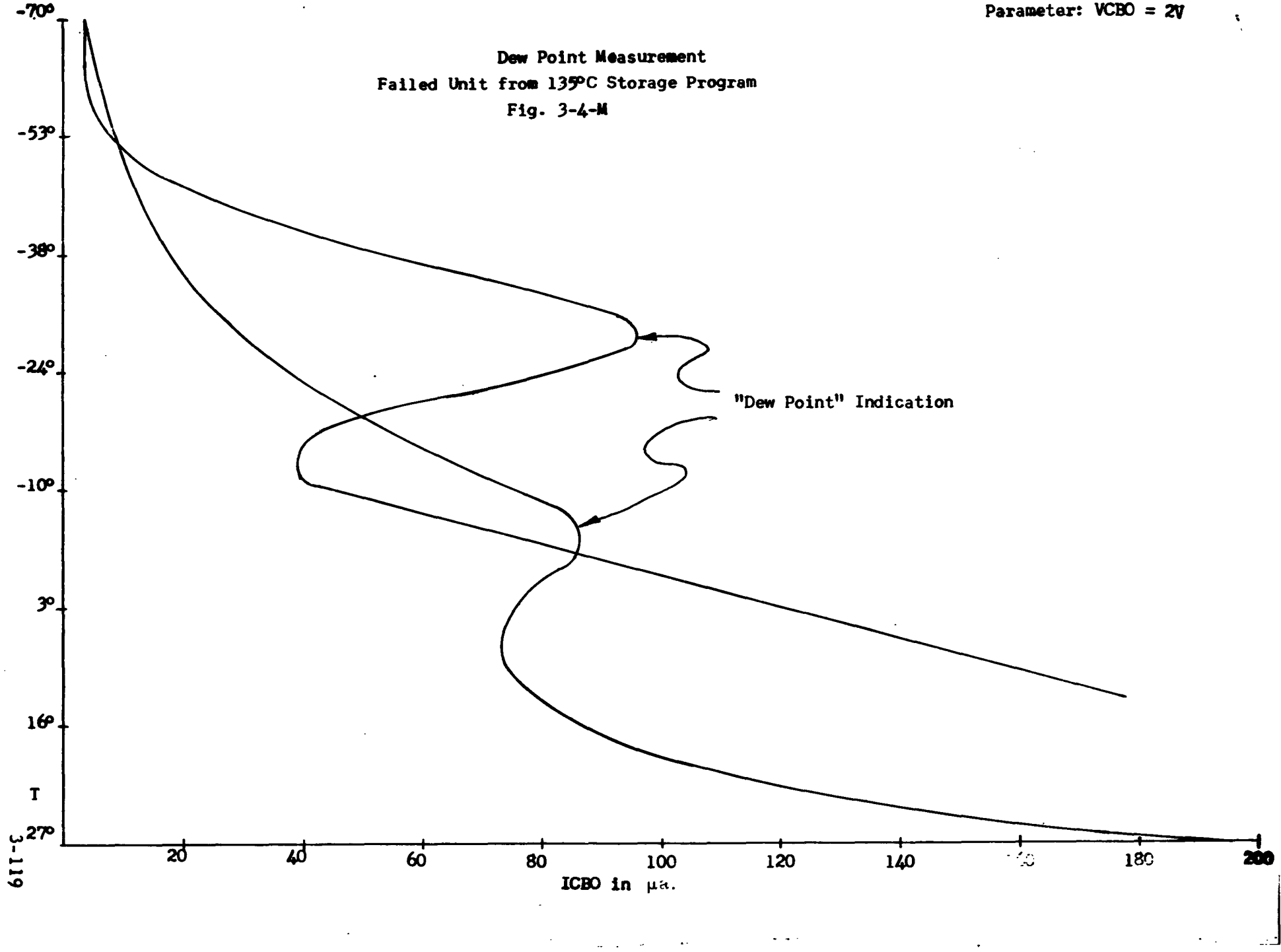
3-118

Dew Point Measurement

Unit Passed on 135°C Storage

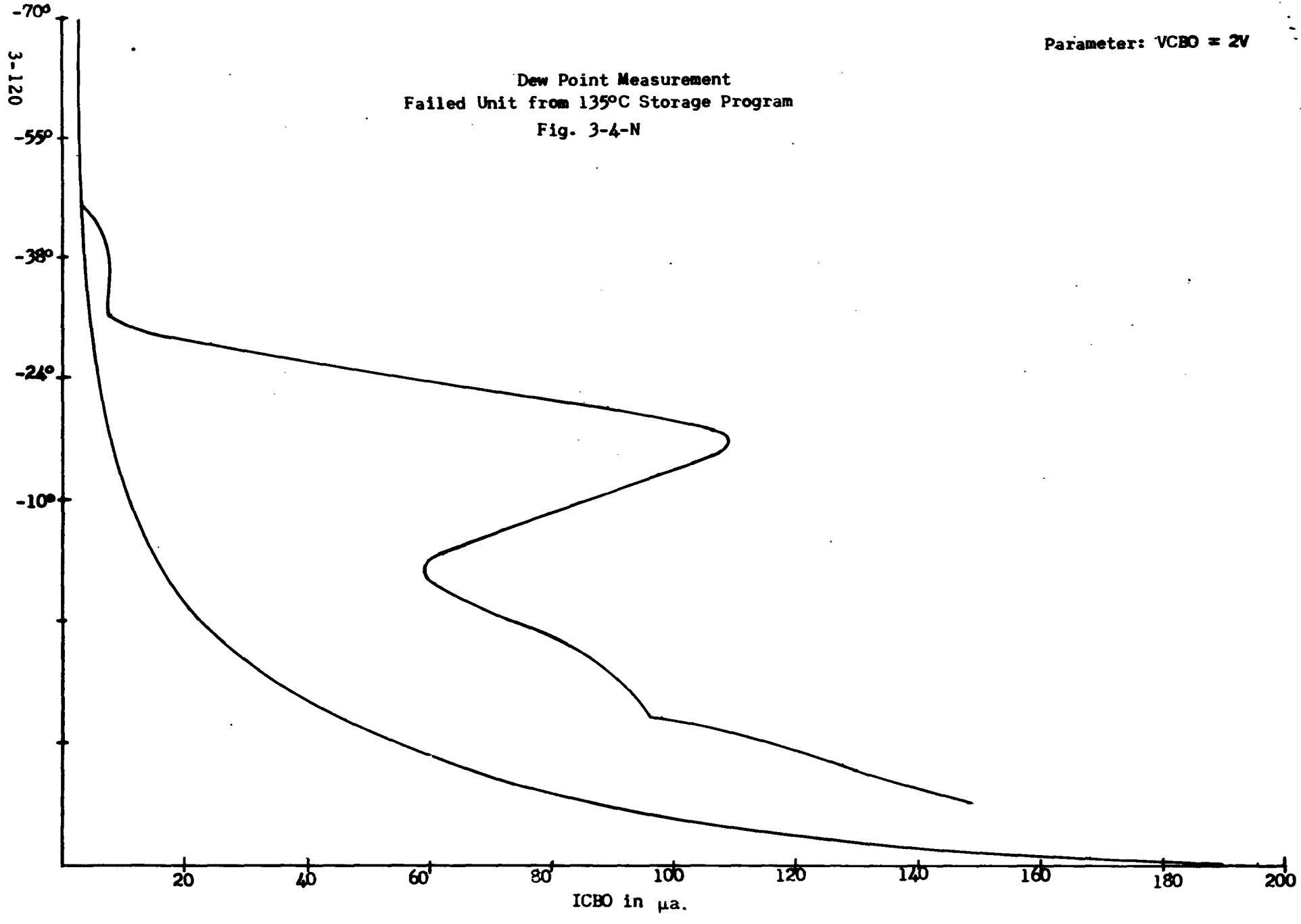
Fig. 3-4-L




Parameter: VCBO = 2V
Dew Point Measurement
Failed Unit from 135°C Storage Program
Fig. 3-4-M
-70°
-53°
-38°
-24°
-10°
3°
16°
27°
T
"Dew Point" Indication
20
40
60
80
100
120
140
160
180
200
ICBO in μa.

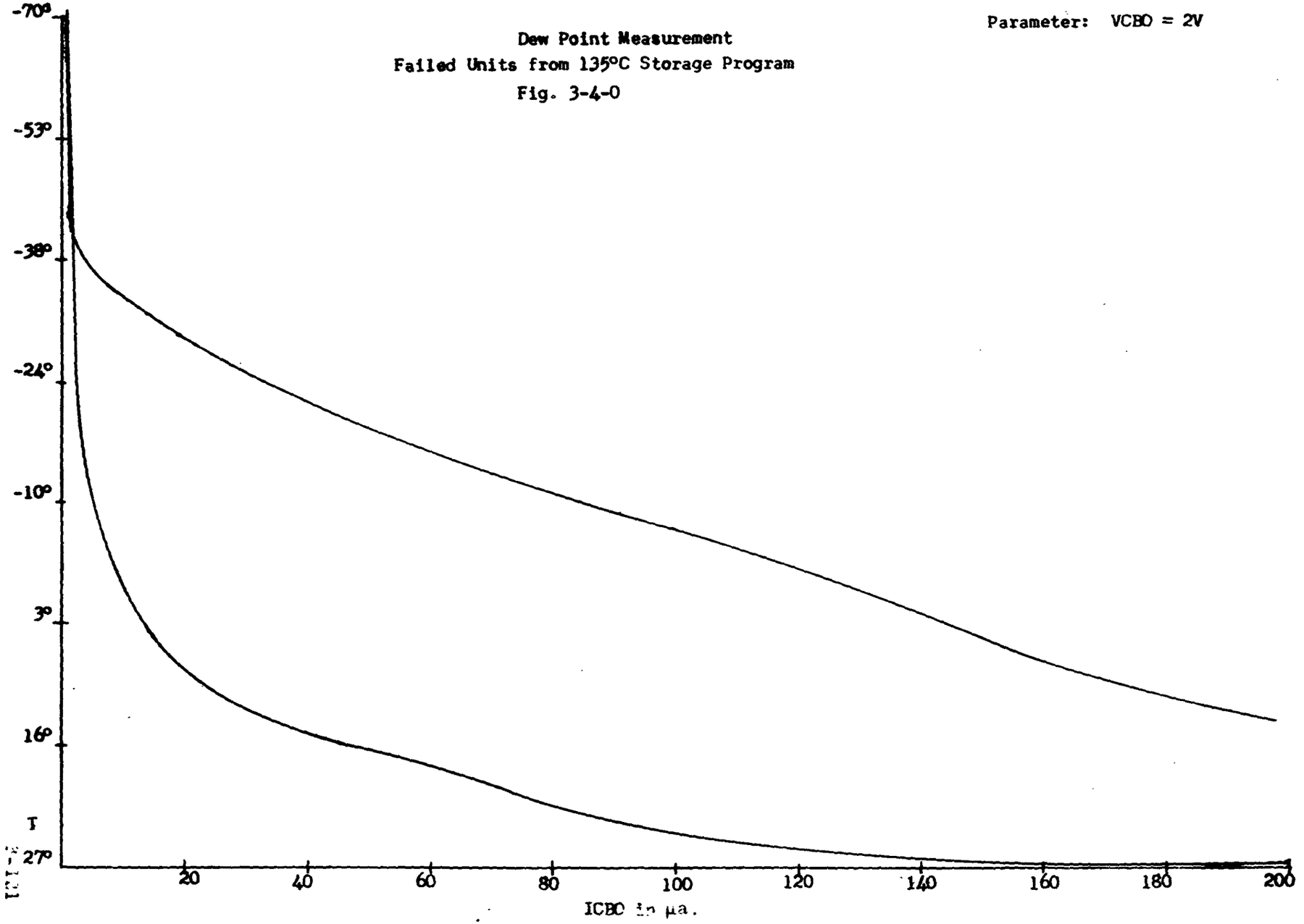
Parameter: VCBO = 2V

Dew Point Measurement
Failed Unit from 135°C Storage Program
Fig. 3-4-N



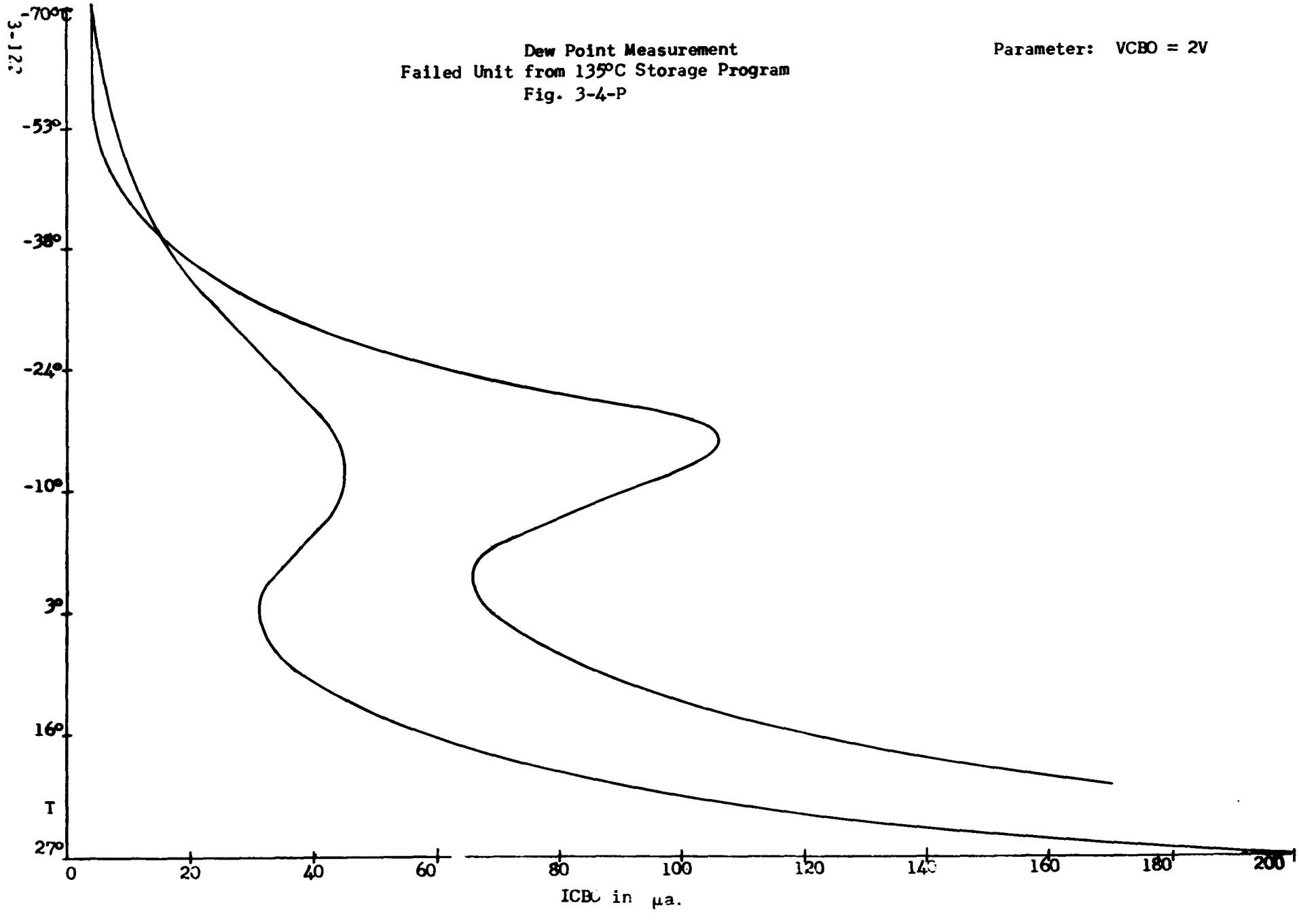
Parameter: VCBO = 2V

Dew Point Measurement
Failed Units from 135°C Storage Program
Fig. 3-4-0



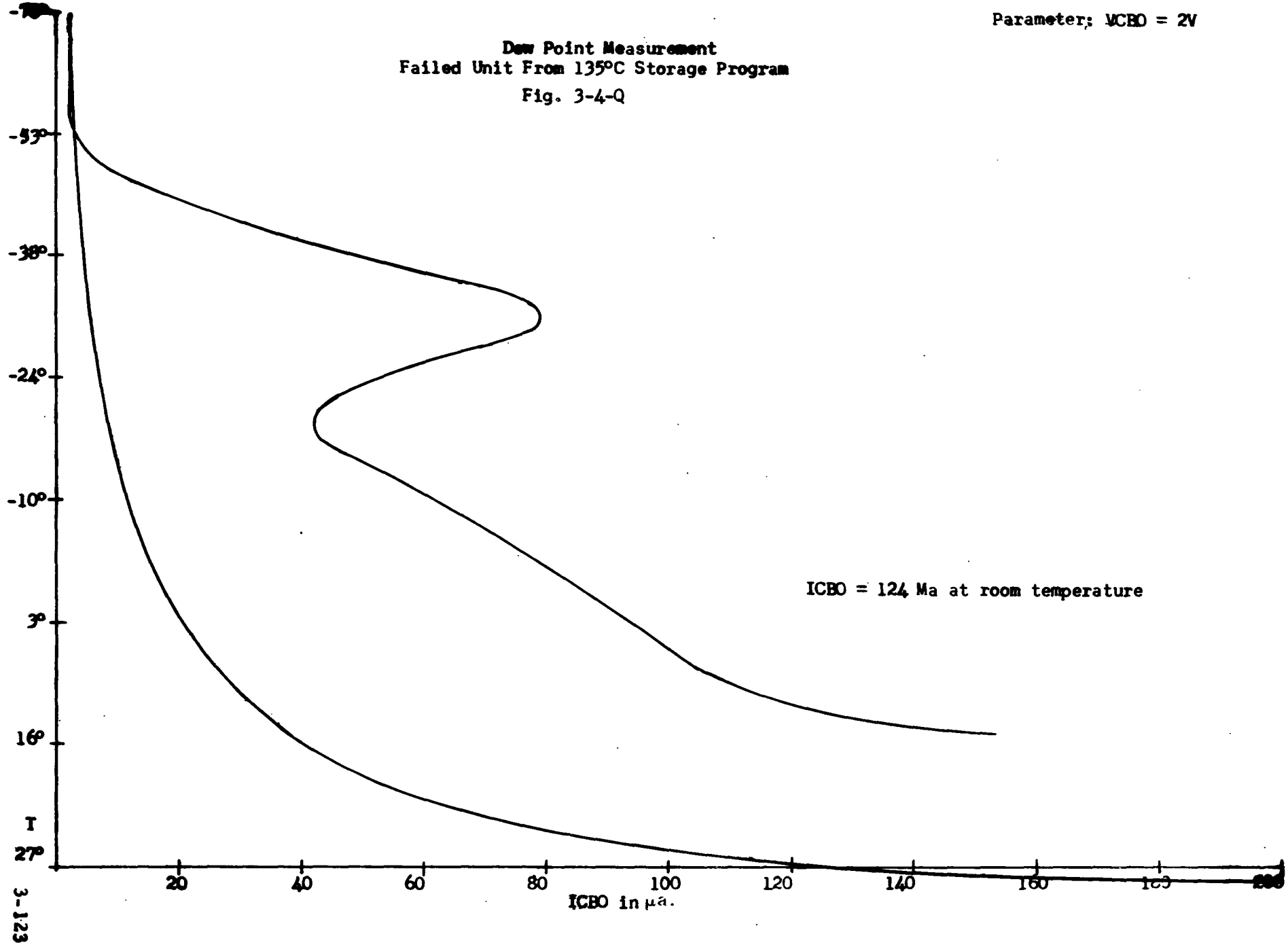
Dew Point Measurement
Failed Unit from 135°C Storage Program
Fig. 3-4-P

Parameter: VCBO = 2V



Parameter: VCBO = 2V

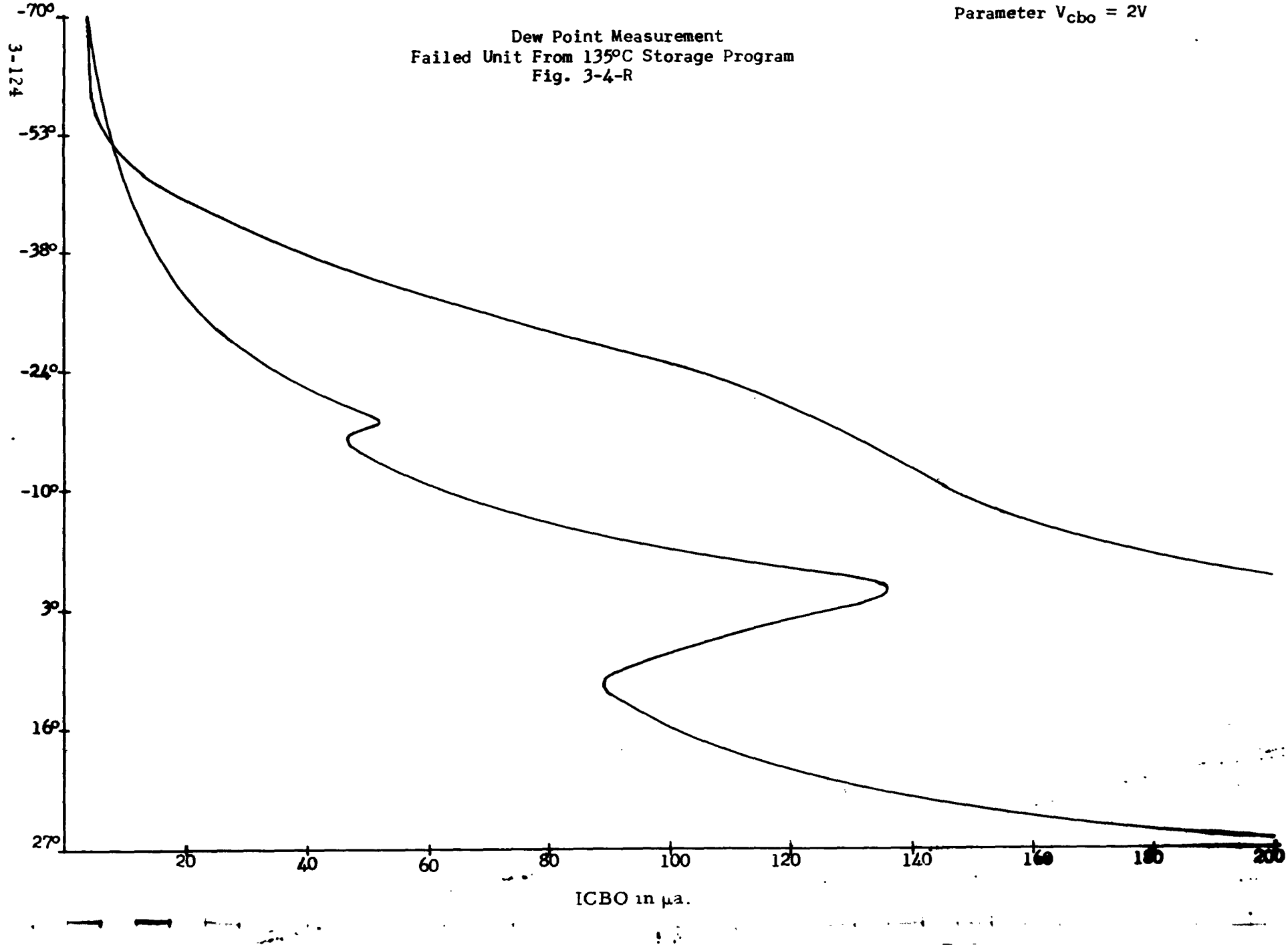
Dew Point Measurement
Failed Unit From 135°C Storage Program
Fig. 3-4-Q



ICBO = 124 Ma at room temperature

Dew Point Measurement
Failed Unit From 135°C Storage Program
Fig. 3-4-R

Parameter V_{cbo} = 2V



of the instrument. An attempt was made to quantitatively assess the moisture content of Units No. 1 and No. 2 of Paragraph 3.4.1B. No difference could be established.

Program for the Next Quarter. Since there has been no success in determining quantitatively a difference in the ambient of failed and satisfactory units, the instrument will be used in the future to study possible sources of ambient contaminates but will not be employed in failure analysis evaluation.

3.4.3 Infrared Spectrophotometer - M. E. Stanton.

A. Colorimetric Analysis Procedure.

General and Engineering Status. Analysis procedure using the spectrophotometer:

The Beer-Bouguer Law may be stated as follows:

$$T_S = 10^{-a_s bc}$$

where T_S = transmittency ratio of the solution to that of an equal thickness of solvent

a_s = absorbancy index

c = concentration of unknown

b = cell thickness

On the double beam instrument $T_S = \frac{I}{I_0}$ is directly recorded.

Interpretation of the analysis is greatly facilitated by looking at a plot of the log of the absorbency versus wave length.

$$A_S = \text{absorbency} = \log_{10} \frac{1}{T_S}$$

$$\log A_S = \log \log \frac{1}{T_S}$$

This can be seen by looking at the log form in detail with two different values of concentration C_1 and C_2, where $C_2 = FC_1$.

$$\log (A_S)_1 = \log a_S + \log b + \log c$$

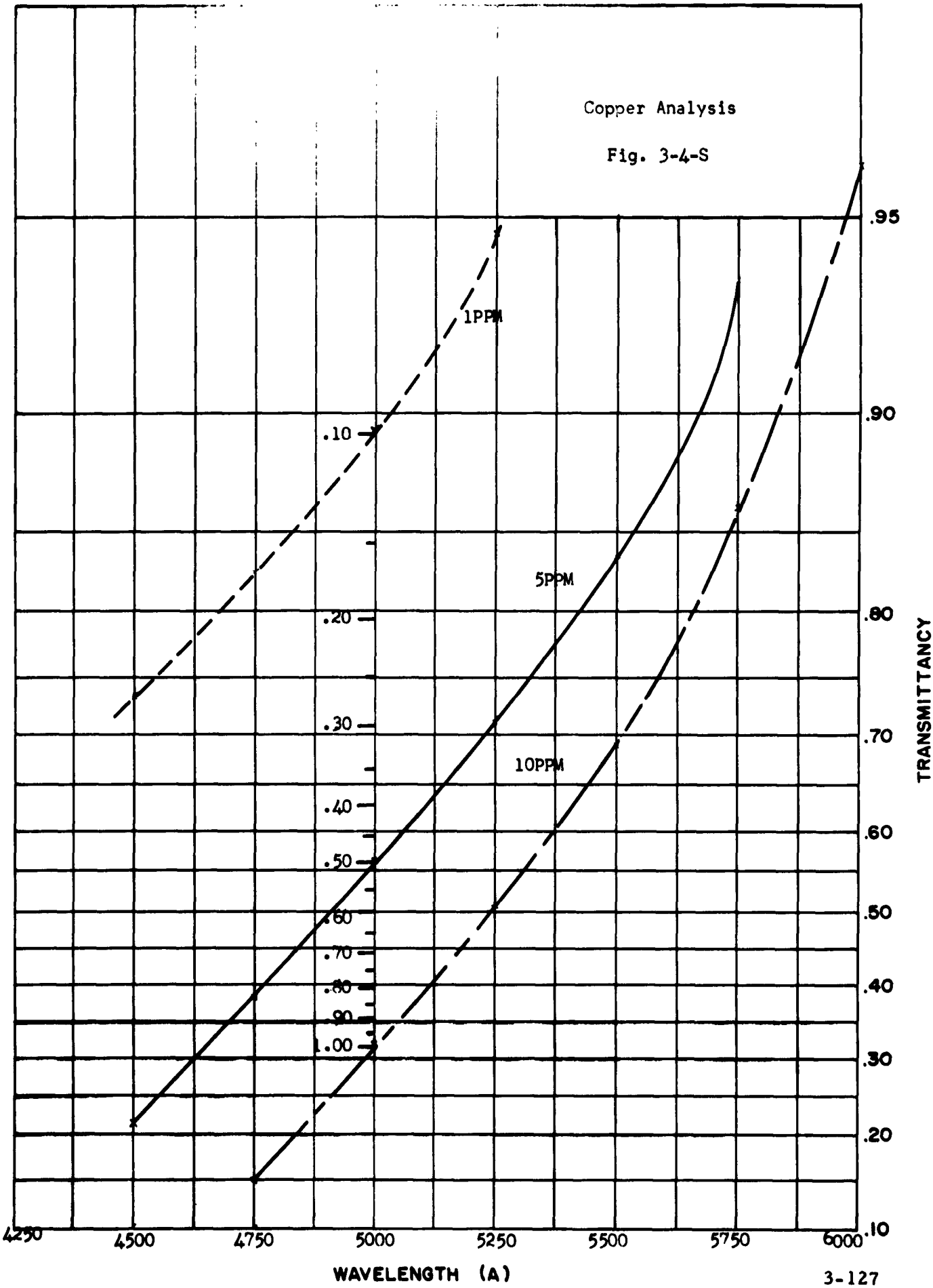
$$\log (A_S)_2 = \log a_S + \log b + \log Fc =$$

$$\log a_S + \log b + \log c + \log F$$

The vertical displacement between the curve for concentration C_1 and the curve for concentration C_2 is equal to log F, and F is equal to the relative concentrations.

a_S for a given solution is a function of wave length, and so it is also seen that curve shapes can be directly compared for qualitative information.

Figure 3-4-S shows an analysis of Cu at 5 and 10 ppm. The graph paper is constructed so that T_S is displayed on the vertical axis and wave length is displayed on the horizonal axis. The vertical scale is construced by plotting log T_S on log paper. With such a scale, it is seen that log A_S will increase from top to bottom.


Copper Analysis
Fig. 3-4-S
1PPM
5PPM
10PPM
.10
.20
.30
.40
.50
.60
.70
.80
.90
1.00
.95
.90
.80
.70
.60
.50
.40
.30
.20
.10
TRANSMITTANCY
4250
4500
4750
5000
5250
5500
5750
6000
WAVELENGTH (A)

By constructing a scale using the same log paper used in the construction of the T_S axis, but increasing from top to bottom, it is possible to take the antilog of log F graphically and arrive directly at relative concentrations. One on the scale is placed on the curve of concentration Fc and the relative concentration of the curve of concentration c is given directly. In the example, F is equal to 1/2 since c = 5 ppm. and Fc = 10 ppm.

To obtain reproducible results, it is important that instrument errors, the validity of the $T_S = 10^{-a_s bc}$ relationship, pH, interfering ions, completion of colorimetric reaction, photo reduction of the solution, temperature, turbidity, loss of ions through plating, and solution of fluorescence, be considered. Each of these topics is treated in detail in Reference[1].

Chemical procedure for copper analysis:

A 100 ppm. solution was prepared by the following procedure:

a) Dissolving .100 gr. of high purity copper in 10 ml. of $HN0_3$ (1:1).

b) Add 15 ml. of HCL 0_4 and evaporate to fumes.

c) Cool - add 50 ml. of water - digest until the salts are dissolved.

d) Cool - dilute to 1 liter and mix.

e) To form the 10, 5, and 1 ppm., dilute volumetrically to the desired solution.

[1] Mellon, M. G., Analytical Absorption Spectroscopy, John Wiley & Sons, 1957.

The formation of the colorimetric solution was accomplished by adding equal quantities of the sample solution and each of the reagents which are as listed:

1. Hydroxylamine Hydrochloride - 100 g/liter water
2. Sodium citrate - 300 g/liter water
3. Neo-Cuproine - 1 g/liter absolute alcohol

This solution was then placed into a glass sample holder 10 cm. in length. This length was determined as being the proper length for the range of detection used, so that T_S falls in the range of 10-90%.

Using this procedure, copper concentrations to .5 ppm. can be quantitatively measured.

Chemical procedure for nickel, lead, and iron analysis:

A 100 ppm. solution has been prepared for each of the named metals by the same procedure as was the standard copper solution.

The reagents for these tests are in stock. Due to the characteristics of some of the reagents, it is advisable not to make up the reagents until the time of test.

The basis for each metal colorimetric analysis was taken from "Spot Tests in Inorganic Analysis" by Feigl. The particular tests are listed below:

1. Copper - Page 91 - Test # 9

2. Lead - Page 74 - Test # 3
3. Nickel - Page 152 - Test # 2
4. Iron - Page 161 - Test # 2

The copper analysis has been used to monitor the copper content in process solutions. The copper content in the KOH etch has been found to increase approximately linearly with the number of processed units. With the scheduling of KOH changes now used, the level is below 2 ppm., immediately prior to the changing of the etch.

The process wash solutions have been examined and no detectable amount of copper was present.

B. Infrared Analysis.

General and Engineering Status. Preliminary experiments have been conducted using the thirsty vycor sample collector technique described in the first Quarterly Report.

Transmission of the sample collector disc has been studied, while distillation of absorbed materials progressed. Because of the temperature limitation of the distillation apparatus, the I. R. adsorption due to H_2O could not be lowered to a level which permitted study of other absorved materials. Before a new distillation apparatus is constructed, the General Motors Research Center will be consulted to determine if water masking is a fundamental limitation on the technique.

Program for the Next Quarter. The consultation mentioned will be done by November 15, 1962, and appropriate review of the critical path plan will be made.

3.4.4 Polarigraph - M. E. Stanton.

Program for the Next Quarter. The polarigraph will be applied to process solutions to determine if this method of analysis has application in the unknown analysis and quantitative control of process solutions.

3.4.5 Electron Probe Microanalyzer - Final Report by Battelle Memorial Institute.

The following is a summary report of our investigation of impurity segregation as possible causes of failure of germanium transistors.

These failures occur as either a collector diode failure or as a recombination failure and result in diode degradation, sometimes to the extent of causing a direct short circuit and local melting of the germanium wafer. There has been some indication that the presence of water vapor may accelerate these failures and that in some cases a degree of recovery can be effected by reverse biasing of the transistor. It has been suggested that these failures may result from impurity diffusion over the surface of the germanium wafer with subsequent precipitation, along low-angle grain boundaries or other imperfections. In an attempt to confirm this proposed mechanism of failure and identify the impurity element(s), a number of transistors have been examined microscopically by electron-probe microanalysis, emission spectroscopy, and X-ray diffraction.

Experimental Work and Results. A number of transistors were specially prepared with a section of the base ring removed to

facilitate examination by electron-probe microanalysis. These samples represented various defects in the germanium wafers and various surface treatments. A list of these samples and their description is given in Table I. Four of these samples were prepared to contain a low-angle grain boundary but the boundary was not delineated by the fabrication process and could not be identified.

Table I. Transistor Samples Prepared for These Investigations.

Sample Number	Description	Surface Treatment (c)
1	Mechanically induced defect	1
2	Ditto	1(a)
3-1	Low-angle grain boundary	1(a, b)
3-2	Ditto	1(a)
4-1	"	2(a)
4-2	"	2
5-1	No grain boundary	1
6-7	Ditto	1
6-8	"	1
6-9	"	1
6-2	"	2(b)
6-3	"	2(b)
6-4	"	2(b)
6-5	"	2(a)
6-6	"	2
11-2	"	3(a, b)
11-3	"	3
11-4	"	3
12-2	Without 135°C storage	3(a)
12-3	Ditto	3(a)
12-4	"	3(b)
23-53	Failed during 135°C storage	1(a)
23-68	Ditto	1(a)

(a) Specimens contained by electron-probe micro-analysis.

(b) Specimens containing interference film contaminant.

(c) Surface treatment:

1. Etched before mounting
2. Etch after mounting
3. Etch after mounting (chemically oxidized)

Microscopic examination at low mangification showed that a few of the samples had films on portions of the germanium wafer which were visible because they were in the thickness range to exhibit interference colors. All of the samples showed a dendritic structure on top of the emitter ring where the ring had been wet by the indium solder.

Electron-Probe Microanalysis. The samples examined by electron-probe microanalysis are indicated in Table 1. The germanium wafers were removed from the base by carefully heating to the melting point of the indium solder. Each of the samples were analyzed for Ni, Co, Fe, Mn, Cu, Zn, Ga, and Pb. No detectable amounts of these elements were found to be present on the surface of the wafer, remote from the base and emitter rings. The sensitivity of these analyses is estimated to be about 0.01 w/o* to 0.03 w/o. It was found, however, that the sensitivity for silver in the presence of germanium was quite low ($\simeq$5 w/o) and was not included in most of the analyses.

* weight percent

Analysis of the dendritic structure on the emitter rings showed indium plus copper. The concentration of copper ranged from 5 w/o to 30 w/o in various portions of the structure. Analysis of the indium solder itself, remote from this structure showed approximately 5 w/o silver and 0.5 w/o copper.

It was observed that when samples containing surface contamination in the form of films showing an interference pattern were introduced into the vacuum of the microanalyzer, the films were apparently removed. As a result of this observation and the apparent negative results obtained by electron-probe microanalysis, it was mutually agreed that additional efforts to identify this material would be made using methods which would not require the sample to be examined in vacua.

Microchemical Analysis. Four samples, in addition to those examined by electron-probe microanalysis, were found to show interference films. Of these samples, 6-2 and 6-3 showed a considerable amount of the contaminant as well as quantities of small crystals, apparently associated with the interference film. Samples 6-4 and 12-3, which contained lesser amounts of the contaminant, were subjected to microchemical spot tests for Ag-Pb and for Cu. These tests indicated the presence of copper in the film on Sample 12-3 and either silver or lead in a similar film on Sample 6-4. The reagents used in making these tests* were:

Ag-Pb: 6:1 Diphenylthiocarbazone and Na_2CO_3 in H_2O.

Cu: Dithio-oxamide (Rubeanic Acid) in alcohol.

* The procedures and reagents used in making these tests are described by F. Feigl, Spot Tests, 4th Edition, Elsevier Press, Houston.

There was not a sufficient amount of material on either sample to allow both tests on each sample.

Emission Spectrographic Analysis. Spectrographic analysis was made of a fragment of the wafer of Sample 6-3, which contained a quantity of the contaminant material. Analysis was also made of a fragment of the same wafer which appeared free of the contaminant. The wafer fragment which contained the contaminant showed the presence of copper, indium, and silver while no detectable amounts of these elements were found in the control specimen. Spectrographic analysis was also made of the indium solder and of the precipitated germanium cyrstals found in the indium solder. The results of these analyses are shown in Table 2.

X-ray Diffraction Analysis. Two samples of material from Sample 6-2 were obtained for diffraction analysis by gently washing the wafer with ethyl alcohol and de-ionized water. Material was also collected from the remainder of Sample 6-3 by washing in de-ionized water. After drying at room temperature, the residue obtained from Sample 6-2 contained a material which appeared fibrous and wax-like. The bulk of this material was found in the residue of the alcohol extraction. The X-ray diffraction patterns all showed germanium plus at least one unidentifiable phase. Both the alcohol and water extractions of Sample 6-2 were found to contain sodium chloride and indium. Cuprous bromide, which was initially reported, has the same structure as germanium and has nearly the same lattice parameter and cannot be distinguished from germanium in these analyses.

Table 2. Spectrographic Analysis of Various Portions of Sample 6-3.

	Ge	Cu	In	Ag	Pb	Sn	Ga
Contaminated wafer fragment	P	P	P	P	-	-	-
Clean wafer fragment	P	-	-	-	-	-	-
Indium solder*	0.05	0.005	100	10	-	0.1	0.1
Germanium crystals*	100	0.1	-	10	-	-	0.1

*Estimated relative amounts present; P indicates present.

Discussion. Both spectrographic and microchemical analysis have indicated the presence of copper and silver in the observed contamination films. Although no compounds of these elements were found by X-ray diffraction, all three diffraction samples showed germanium. It is possible that copper and silver are in solution with small crystallites of germanium on the surface of the wafer. It cannot be stated with certainty that the copper and silver are components of the interference films or whether the interference films are associated with small crystallites of germanium remaining on the surface of the wafer. Although the observed interference films are extraneous, it should be noted that none of these films were observed on components that had actually failed.

The negative results obtained by electron-probe microanalysis tends neither to confirm nor reject the initially proposed mechanism of surface diffusion and subsequent grain boundary diffusion. If such a mechanism were operative, distribution of an impurity element over the surface would most likely occur during the alloying diffusion anneal. Subsequent etching of the surface would remove the impurity from the surface but may not remove impurities that have already reached an imperfection.

3.4.6 Surface Coatings - R. P. Anjard.

General and Engineering Status. Adsorbed gas atoms on a semiconductor surface [1, 2] are similar to impurity atoms in that they cause localized electronic states. [3] Considering the effects of surface states, their occupancy will be determined by the position of the Fermi level. These states may be either positive or negative. The total charge in the various surface states will determine the direction and amount that the energy bands at the surface are changed. In Figure 3-4-T, the energy structure [4, 5] is shown for an N-type accumulation layer. This is a common energy configuration for the case of adsorbed water. A surface potential ϕ_s is defined as the difference between the Fermi level and the bulk intrinsic Fermi level at the surface.

1 N. F. Mott, Proc. Inst. Electrical Engineer, 96, 253, (1949)
2 N. Cabera & N. F. Mott, Repts. Prog. Phys., 12, 163 (1949)
3 H. Statz, G. deMars and others, Phys. Review, Vol. 101, No. 4, 1272-1281 (1956)
4 G. deMars, Semiconductor Products, 24-28 (April, 1959)
5 R. H. Kingston, Phys. Review, 98, 1766-1775 (1955)

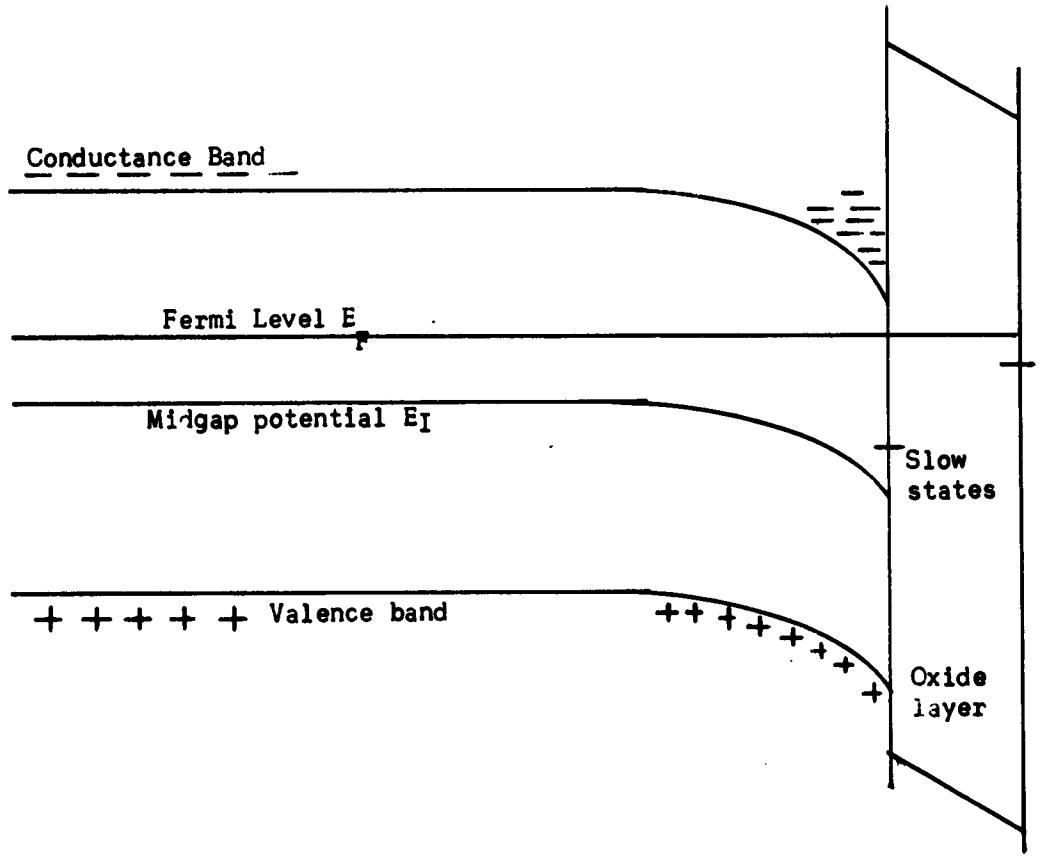


Fig. 3-4-T

Energy band structure at semiconductor surface--oxide surface is positively charged.

Water vapor generally causes substantial degradation of the transistor characteristics.[6-13] It is, therefore, desirable to exclude moisture from the germanium surface after final surface treatment and encapsulation. The sources of this moisture are (1) the encapsulating ambient itself; (2) outgassing from the internal surfaces, particularly, the nickel plating; and (3) the germanium surface itself.[14] As stated in the contract proposal, Delco and others have had success with small devices and with experimental power devices using silicone-resin coating materials to provide a surface which is impervious to moisture. The suppliers of these compounds have improved the purity, viscosity control, and moisture content to the point that it is practical to reconsider their usage for the 2N1358 and other power devices.

The series of various varnish experiments is identified as Group 1 in the Data Summary Table, 3-4-U. The individual experiment procedures are described:

1-1. Dow Corning's Sylgard 182 was applied to 28 2N1358 basic units, after a precap bake of 1 hour at 130°C. The application was performed in a dry box controlled to -50°C, maximum. After curing 96 hours at 120°C, the devices were reintroduced into the production line and capped. The entire element was covered.

6 A. J. Wahl & J. J. Kleimack, "Proceedings of the IRE," Vol. 44, pp 494-502 (April, 1956).
7 J. T. Law, Proc. Inst. Radio Engrs., 42, 1367 (1954)
8 J. T. Law & P. S. Meigs, J. Appl. Physics, 26, 1265 (1955)
9 E. N. Clarke, Phys. Rev., 99, 1899 (1955)
10 Eriksen, Statz & deMars, J. Appl. Physics, 28, 133 (1957)
11 A. R. Hutson, Bell Telephone Monograph Series, 1956
12 W. H. Brattain & J. Bardeen, Bell System Tech. J., 32, 1 (1953)
13 R. H. Kingston, Phys. Rev., 98, 1766 (1955)
14 J. T. Wallmark & R. R. Johnson, RCA Review XVIII, 4, (December, 1957)

1-2. The varnish and application technique were the same as 1-1. However, the transistors were previously chemically oxidized.

1-3. Dow Corning's XR6-1043 semiconductor coating resin is one of the purest varnishes available. After the precap bake, units were coated such that the entire element was coated as in 1-1 and 1-2. As the suggested curing cycle, 3 hours at 200°C, could not be considered, the cycle selected was 96 hours at 120°C. XR6-1044 and XR6-1045 which can be cured at lower temperature were not considered due to the addition of catalysts. After curing, the parts were transferred to the production facilities and encapsulated.

1-4. This experiment using chemically oxidized elements has the same relation to 1-3 as 1-2 did to 1-1.

1-5. 2% A_s (which will be explained later) was added to XR6-1043. However, the powder was fairly coarse. Also, it was difficult to maintain a homogeneous mixture due to the settling of the arsenic trioxide. The basic treatment outlined in 1-3 is applicable; however, only the emitter was coated.

1-6. This is basically a control group and was precap baked 1 hour at 130°C and 96 hours at 120°C. This group was processed with 1-1 through 1-5, inclusive.

1-7. After a 1 hour precap bake at 130°C, radio grade units were extracted from the production line and allowed to cool in a desiccator, and then 20 minutes at 40°C in a dry box controlled to a -80°C dew point. After coating, an additional 30 minutes in this dry box was allowed for slow evaporation of volatiles, and the units were baked 2 hours at 135°C under a slight vacuum (1000 microns). They were transported via desiccator to the production line, baked, and encapsulated.

1-8. 2N1358 type units were processed as in 1-7. The whole element was also coated.

1-9. 2% arsenic was added to the SR98 and applied to units as in 1-8. A limited sample size, 7 pieces, was used. The same problems existed as in 1-5.

1-10. This experiment was the same as 1-9, except that the varnish was applied to the emitter only. This was an attempt to reproduce the high gain observed in experiment No. 1-5.

The application of such coatings to the emitter junction only is particularly attractive because the considerations for maximum collector diode breakdown voltage and minimum emitter recombination current are not compatable. The diffusion current to surface recombination sites (mostly around the emitter as shown in Figure 3-4-V of 3.4.7) is less with an accumulation layer because of the drift field presented to minority carriers. Also, as the surface Fermi level is changed, the effectiveness of surface sites for the recombination process is changed, as shown

in Figure 3-4-W of Section 3.4.7. The accumulation layer at the surface on the emitter side then seems desirable. Since the diode breakdown has been shown to be a surface avalanche phenomena, an inversion layer will result in a greater field at the surface termination of the junction; and, hence, a lower voltage breakdown. This is not desirable on the collector diode. According to J. J. A. Ploos van Amstel [15], arsenic as a donor element makes the surface more N-type; and, thereby, creates a layer similar to that caused by water vapor.

Conclusions. The results are outlined below:

a. Experiments 1-3 and 1-4 exhibited significant diode degradation during aging, such that 100% failures occurred.

b. Experiment 1-5 exhibited a very high gain after aging.

c. The data for 1-5 in Table 3-4-U shows continual degradation of the uncoated collector diode during storage at 135°C. All units were rejected after four weeks storage.

d. The failures of Groups 1-3, 1-4, and 1-5 were attributed to incomplete curing.

e. On production units coated with Sylgard 182, the diodes improved to a limit and remained relatively stable through the 1000 hours at 135°C. The gain variation was ± 3.8% using the aged units as the base.

15 J. J. A. Ploos van Amstel, Phillips Technical Review, 22, 204 (60/61).

Experiment No.	Experiment Description	ICBO After Cap	ICBO After Age	ICBO 2	ICBO 4	ICBO 6	ICBO A/C	ICBO A/A	IEBO 2	IEBO 4	IEBO 6
1-1	Sylgard 182	1.35 (2.8)	.53 (.51)	.41 (.37)	.39 (.37)	.39 (.38)	.94 (2.1)	.50 (.57)	.27 .29	.64	.23 (.27)
1-2	Chemically Oxidized with Sylgard 182	1.62 (1.5)	1.31 (.91)	1.38 (1.0)	1.98 (1.1)	2.70 (3.3)	1.72 (.66)	2.20	1.25 (.6)	1.43 (1.2)	1.40 (1.30)
1-5	XR6-1043 AS/emitter	.61 (.76)	.42 (.39)	4.7 (8.6)	750						
1-6	Baked 97 Hours	1.27 (2.2)	.90 (1.0)	.78 (.93)	.85 (1.0)	1.14 (1.3)	.75 (.74)	.64 (.63)	.31 (.28)	.26 (.28)	.35 (.31)
1-7	SR98	1.22 (1.03)	1.13 (1.0)	.99 (.83)		.91 (1.19)	.52 (.7)	.48 (.71)	.45 (.62)		.60 (.79)
1-8	SR98	2.32	2.28	1.41 (.82)			.74	.79	.82 (.99)		
1-9	SR98 AS/ on entire element	1.21	1.1	.75 (.35)			1.35	1.25	1.15 (.50)		
1-10	SR98 AS/ on emitter	1.76 .96	1.79 (1.0)	2.29 (1.40)			1.30 (.87)	1.28 (.98)	1.18 (1.28)		

NOTE: ( ) - Standard deviation of parameter

		IB_2					2 Volt		Diode			Number Units	Failure Report Failures Determined in Nth Week			Failure Rate /1000
4	6	A/C	A/A	2	4	6	A/C	A/A	2	4	6	After Age	2	4	6	Hours
.64	.23 (.27)	194.8 (19.3)	212.4 (24.9)	220.5 (19.5)	202.5 (22.4)	204.9 (22.4)	108.7 (16.9)	94.7 (14.0)	124 (16.2)	62.3 (8)	65.8 (14.6)	21	0	0	0	4.75
.43 .2)	1.40 (1.30)	104.1 (9.1)	106.4 (11.0)	104.6 (11.3)	102.7 (11.4)	111.1 (13.8)	82.1 (17.6)	59.5 (10.5)	57 (10.7)	74.4 (17.0)	66.9 (13.8)	8	1 Vf1	0	0	N/A
.26 .28)	.35 (.31)	239.8 (17.9)	231.3 (20.8)	212.6 (23.4)	209.7 (25.7)	217.1 (24.2)	102.5 (11.8)	101.4 (12.4)	80.6 (10.6)	64.5 (13.0)	68.1 (10.9)	18	1 Vf1	0	0	11.5%
	.60 (.79)	124.0 (30.0)	161.8 (48.0)	172.7 (39.5)		170.5 (40.5)	72.4 (10.1)	91.9 (16.6)	135.8 (25.6)		110.8 26.7	22	1 Vf1 2V	1(2V)	1 (2V)	22.7%
		144	200	234.1			119	76	114 (20.7)			13	1 Vf1 0	0	0	
		146	171	206.5			114	65.5	75.5 (9.2)			2	0	0	0	
		152.6 (33.6)	180.6 (29.4)	213.4 (26)			77.8 (20.6)	(55.8) (9.9)	84.2 (14.2)			28	0	0		

FIGURE 3-4-U

NOTES

1. Gain rejects have not been dropped thereby providing a more complete understanding of the effects of the treatments.
2. V_{F1}, 2V, I_{CBO} and I_{EBO} are the parameters for which the failure rates have been computed.
3. The two experiments dropped utilized DCX6-1043 silicone varnish.

f. The chemically oxidized units coated with Sylgard 182 maintained their high and stable gain characteristics throughout the 1000 hours. Although the emitter and collector means were significantly greater than their counterpart, 1-1, no diode failures occurred.

g. Experiment 1-6 might be better classified in the precap bake group, but as a control will be analyzed at this point. The collector diode mean continued to increase while the emitter diode approached a minimum limit. The gain was initially low, but during aging tended toward a higher gain limit. This final failure was typical for devices precap baked 15 minutes, 45 minutes, and 1 hour.

h. Experiment 1-7 - the diodes were relatively stable during storage. The gain reached a limit before 336 hours at 135°C. It must be reiterated that these units are radio grade and were not tested to the 2N1358 limits.

i. Experiments 1-8 through 1-10 have only completed 4 weeks storage at 135°C. The high gain anticipated by the suspension of arsenic trioxide in the varnish was not obtained. This experiment will be repeated.

Note:

a. Groups 1-1, 1-2, 1-6, and 1-7, are being tested under modulation life conditions.

Program for the Next Quarter. The analysis of the experimental data is near completion. During the next quarter, some of the experiments will be repeated, and further analysis will be made.

3.4.7 Precap Aging and Desiccant Experiments - R. P. Anjard.

General and Engineering Status.

Oxide Formation: Germanium, unless it has not been exposed to oxygen, is covered by an oxide film. [1] Thus, there is a true surface on the oxide and an interface between the bulk material and the oxide. If the two lattices do not join continuously, lattice defects may be located at the interface which result in localized states. According to one oxidation theory, [2] there should be vacancies in the surface layer of the semiconductor which are the result of atoms pulled into the oxide film under an electrical field. This field is suggested to be caused by negative oxygen atoms on the oxide surface. The oxide film, however, may be imperfect and have interstitial semiconductor atoms which should be mobile.

The adsorption of the first oxygen, which may adsorb as O^- may generate acceptor states in which the hole is more weakly bound and therefore allow a greater fraction of holes to ionize from the surface. In a second mode of adsorption, the oxygen may bond to the germanium as a peroxide by filling the unfilled orbitals of two germanium atoms and thereby removing two surface states. [3] Recent Soviet tests on the effect of atmospheric oxygen on the surface of germanium showed that oxygen reacts

[1] H. Statz, G. A. deMars, L. David, A. Adams, Phys. Review, 101, 1272 (1956).
[2] N. Cabrera and N. F. Mott, Reports Prog. in Phys., 12, 163 (1949).
[3] Handler, Semiconductor Surface Physics, Univ. of Penn. press (1957).

to form a non-metallic film that is made up of non-volatile oxide and volatile, loosely-bound molecular oxygen.[4] An intermediate layer of peroxide layers is postulated. Its growth can be retarded by a vacuum treatment. This was also stated by Handler.[3] It has been reported by Lanyon and Trapnell[5] that oxygen formed a monolayer of one oxygen atom per surface metal atom, followed by a second monolayer of one to two oxygen atoms per original metal atom. The rate of formation for the second monolayer was found to be proportional to the square root of the oxygen pressure. Experiments[2, 6, 7] concerning the initial stages of oxidation have been supplemented by Ligenza.[8] His work indicates that at 125°C, the maximum amount of oxygen taken up in atoms/cm² can be expressed as: $q = 1.49 \times 10^{14} \log t + 10.3 \times 10^{14}$, where t is time in minutes. Thus, at 125°C within 20 minutes, 3×10^{-8} grams of oxygen/cm² are formed on the surface. There is a small increase between 20 and 60 minutes, and, in general, the oxidation approaches an asymptotic value of approximately 3.82×10^{-8} g of oxygen/cm². It is interesting to note that the logarithmic growth rate is obeyed from 25° to 250°C, up to a coverage of 3.82×10^{-8}g of oxygen/cm²; and that after being exceeded, a new oxidation law is obeyed. This transition appears to have a time-lag associated with it. The time lag could correspond to the time necessary to transform a layer of oxygen atoms chemiadsorbed to a monolayer of germanium dioxide "molecules." The observed time lag was between 100 and 140 minutes at 125°C.

It has been established that the oxide formed is porous and that the depth of adsorption of water vapor may vary from 2-10

[4] Breakthrough, United Carbon Products Co., Vol. 3-No. 3, March, 1962.
[5] M. Laynon and B. Trapnell, Proc. Roy. Soc., A227, 387 (1954).
[6] M. Green, J. Kafalas, P. Robinson, Ref. 3.
[7] T. P. Wolsky, J. Phys. Chem. Solids, 8, 114 (1959)
[8] J. R. Ligenza, J. Phys. Chem., 64, 1017 (1960).

monomolecular layers. [9] It is well known that the presence of moisture has a marked effect on the reverse current of germanium diodes. [10, 12] It has been established that these changes may be caused by the change in surface recombination velocity, formation of channels and/or ionic conduction in the adsorbed water. The effect of this water vapor or an N type surface was presented in Section 3.4.6.

Semiconductor Surface and Recombination Velocity. The phenomena of surface recombination must be considered when analyzing the affects of ambients, particularly moisture. If free carriers are produced close to the surface, they will diffuse toward the surface and consequently recombine at the surface rather than in the volume. [13] In a filament in the presence of a field, the current has components which represent a diffusion current. The current toward the surface is:

$$I_y = I_Z = \pm qs\delta p \qquad (1)$$

where s has the dimension of velocity and is called surface recombination velocity and δp is the excess carrier concentration. The expression for surface recombination for a single level is: [14]

$$S = C_p C_n N_t (P_o + n_o) \left[C_n (n_s + n_{s_1}) + C_p (P_s + P_{si})\right]^{-1} \qquad (2)$$

where n_s, P_s = free carrier densities at the surface
n_{s_1}, P_{si} = surface carrier density when $Ep = E_s$
N_t = number of surface states present

[9] J. T. Law, J. Phys. Chem, 59, 67, (1955)
[10] H. Christensen, Proc. Inst. Radio Engr., 42, 1371 (1954)
[11] J. T. Law, Proc. Inst. Radio Engr., 42, 1367 (1954)
[12] A. L. McWhorter and R. H. Kingston, Proc. Inst. Radio Engr., 42, 1376 (1954)
[13] G. Bemski, IRE (1958)
[14] D. Stevenson, R. Keyes; Physica, 20, 1041 (1954)

C_p, C_n = capture probabilities of holes and electrons, respectively
P_o = density of holes in the valence band
N_o = density of electrons in the conductor band

In many experimental techniques, the properties of the surfaces have been measured - such as the surface conductance, inversion layers,[14-22] contact potential and surface recombination velocities, as a function of ϕ_s. The actual description of recombination at the surfaces involves several levels. Fast states which exist near the center of the gap act as acceptors.[22] Statz reported levels in germanium at 0.14 e.v. below the middle of the gap. Another group of states, called slow states, exhibit long decay times.[23] These states are responsible for the variation of ϕ_s with the ambient gases.

In Figure 3-4-V, a diagram of the current flow lines in a typical alloy transistor geometry is presented. It can be seen that the surface recombination takes place primarily in the annular ring surrounding the circular emitter alloy.[24]

15 G. C. Doamanis, Bull Am. Phys. Soc., Ser. II, 2, 65, 135 (1951)
16 Henisch, Reynolds & Tipple, Physica 20, 1033 (1954)
17 J. Thomas and R. Rediker, Phys. Review, 101, 984 (1956)
18 Many, Margoniski, Hornik and Alexander, Phys. Rev. 101 1433 (1955)
19 W. Brattain and J. Bordeen, Bell System Tech. J., 32, 1 (1953)
20 Many, Hornik and Margoninski, refer referecen 3, page 85
21 G. C. Dousmanis & E. Johnson, Bull Am. Phys. Soc., Ser. II, 2, 170 (1957)
22 C. G. Garrett & W. Brattain, Bell System Tech. J., 35, 1041 (1956)
23 R. Kingston, reference 3
24 L. P. Hunter, Handbook of Semiconductor Electronics, McGraw-Hill Book Company, Inc., (1956) page 4-10.

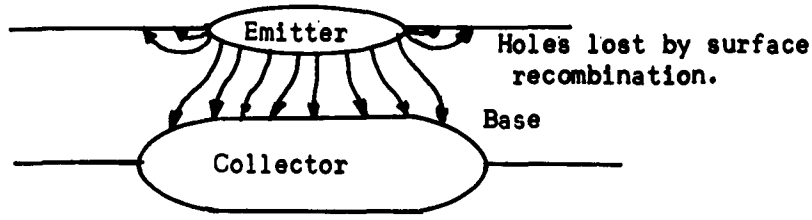


Figure 3-4-V
Diagram of Current Flow in a PNP Alloy Transistor

The dependence of surface recombination velocity, S or ϕ_s has been referred to previously. Depending on the density, energy levels, distribution and carrier capture, cross-sections of the recombination states, curves [25] of the type shown in Figure 3-4-W can be calculated.

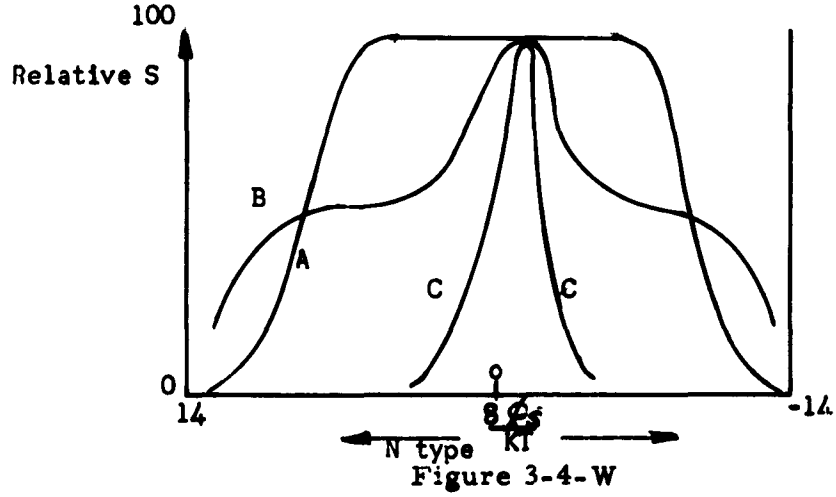


Figure 3-4-W

[25] G. Dousmanis, Phys. Rev., 112, 369 (1958)

Curves of s versus $q\phi_s/KT$ for various distributions of the surface recombination states. A: curve for a single surface state level. B: two energy levels equally effective for recombination. C: continuous distribution of levels.

Margoninski and Farnsworth [26] measured the surface recombination velocity and trapped charge density in the fast states as a function of surface potential on an N type specimen which was subjected to room air vacuum, dry air vacuum, and wet oxygen vacuum. The most important results were that dry nitrogen had no influence on any of the surface state parameters, that dry oxygen affected only the density of states, and the unperturbed surface potential, and that wet nitrogen and wet oxygen had almost the same and most pronounced effect on the fast surface states. It has also been found that for a freshly etched junction when placed in a vacuum, the change is in the direction of increased surface recombination. [27] The addition of water vapor decreased the surface recombination rate, S, which returned to its previous high value on re-evacuation. If heated to approximately 100°C, s increased more rapidly and reached a higher level. Thus, ambients affected the surface states and changed the surface recombination velocity. Changes in surface recombination rate can be observed in the relative values of transistor gain.

Vacuum Treatment. Wahl and Kelimack [28] found that a reproducible set of characteristics can be repeatedly reestablished after water vapor or oxygen had caused a large

[26] Y. Margoninski, & H. Farnswoth, Phys. Rev., 123, 138 (1961)
[27] J. Law and P. Meigs, Bell Telephone Monograph Series (1955)
[28] A. Wahl and J. Kleimack, Proceedings of the IRE, 44, 494 (1956).

change in the characteristics. On a PNP transistor, oxygen caused an increased junction breakdown voltage, increased reverse current and increased gain, while water vapor decreased the junction breakdown voltage, decreased the reverse current to a limit and increased gain. Water vapor decreased breakdown voltage, V_B, because the negative charge induced by the positive ions on the surface caused the surface resistivity of the base region to shift to still lower N types as shown in Figure 3-4-T of 3.4.6. Wahl further reported that the best technique for the removal and exclusion of water vapor and oxygen involved vacuum baking and vacuum-tight sealing; whereby, the atmosphere is inert, i.e., nitrogen, hydrogen, or helium. Evacuation without heating was found to be inadequate because the internal surfaces of the sealed device allowed evolution of water vapor and oxygen, if not precap baked. The principle was referred to in Section 3.4.6. Although very nearly ideal time stability of characteristics were obtained under severe aging conditions by vacuum baking to remove water vapor and oxygen, the transistor surface is extremely sensitive to entrapped moisture or oxygen. Wahl further stated that certain oxides actually reduced the sensitivity to water vapor and oxygen and, if controlled, would be highly desirable. In the reported experiment, transistors were vacuum baked at 135°C in a vacuum which was about 2×10^{-6} mm. Hg. and cooled to room temperature. Although extensive vacuum cleaning experiments have been reported [7, 29, 30] very few were concerned with the practical upper and lower temperature limits.

Controlled Ambient by Desiccants. In addition to the reliability problem presented by the entrapment of moisture, it has been

[29] R. Schlier and H. Farnsworth, reference 3
[30] M. Green, J. Kafalas and P. Robinson, reference 6, page 349.

found that transistors upon removal from elevated temperatures show an increase in gain. The final value is reached after approximately 48 hours. [31] Thus, stability of transistors is another major consideration and ambient control presents greater problems. In 3.4.', three sources of moisture for an encapsulated transistors were presented. Getters have been used in the production of electron tubes to maintain the purity of rare gases or to improve or maintain the vacuum. [32] When a gas or liquid is exposed to a porous adsorbent, a getter, a certain amount of the gas or liquid is sorbed by the solid. The amount of gas or liquid adsorbed when equilibrium is established at some temperature and pressure is a function of both the adsorbent and adsorbate. Surface area, pore size, shape and distribution are all important adsorbent properties. In general, the higher the pressure the more material that will be adsorbed;and the higher the temperature, the lower the adsorption. There are two types of sorption - physical adsorption and chemisorption. The difference is in the magnitude of the forces between the sorbate and sorbent. In physical adsorption, the entire surface is available;while in chemisorption, there are only certain active sides on the sorbent surface. At low partial pressures, the physical adsorption is low, while chemisorption is large.

The major classes of adsorbents in use are aluminum oxide, activated carbon, silica gel, crystalline zeolite (natural and commercial), and thirsty vycor.

Wallmark and Johnson [31] found that transistors encapsulated with a molecular sieve (a commercial zeolite), the shift in the gain was only 3%. Transistors filled with a silicone grease

[31] J. T. Wallmark and R. Johnson, RCA Review, 18, 512 (1957)

[32] M. Knoll, "Materials and Processes of Electron Devices," Spungio-Verlag, Berlin (1959.

mixed with 5% boracic acid exhibited gain stability.[33] Cooper[34] indicated that if a getter preserved a partial water-vapor pressure equivalent to a dew point below the lowest temperature of storage, the moisture will not be detrimental to the device. He further stated that the required dryness for reliability could be preserved in practice only by a getter, and that molecular sieves had many advantages for this purpose. There are certain practical problems involved when considering getters. Activation, driving moisture to a very low level, is not difficult. Maintaining a minimum level at encapsulation, however, can be a serious problem.

Analysis of Getter Types - Molecular Sieves. Of the getters mentioned, commercial zeolites (molecular sieves) and thirsty vycor are the most commonly used in transistor fabrication.

Concerning molecular sieves, the most common types commercially available are Linde 4A, 5A, and 13X. 4A's chemical structure is $0.96 \pm .04\ Na_2O \cdot AL_2O_3 \cdot 1.92 \pm .09\ SiO2 \cdot nH_2O$., and the voids amount to 45% of the volume of the zeolite. Type 5A is similar to 4A, but 75% of the sodium ion was replaced by calcium ion. 13X is $0.83 \pm 0.05\ Na_2O \cdot Al_2O_3 \cdot 2.48 \pm .03\ SiO_2 \cdot n\ H_2O$ and has a void volume of 51%.[35] Figure 3-4-X compares the Linde commercial zeolites with Silica Gel and activated alumina.

Figure 3-4-Y[36] shows that below 35% relative humidity, molecular sieves have a higher capacity than silica gel or alumina.

[33] J. J. A. Ploos van Amstel, Philips Tech. Rev. 6, 204 (1960)
[34] R. Cooper, Proc. IRE, 50, 141 (1962)
[35] Linde Bulletin, F9947-C (1961)
[36] C. Hersh, "Molecular Sieves," Reinhold Publishing Corporation, New York, 1961, page 53.

Fig. 3-4-X

Ref: Molecular Sieves:
Charles K. Hersh
1961, p. 60
and
Corning Glass Works

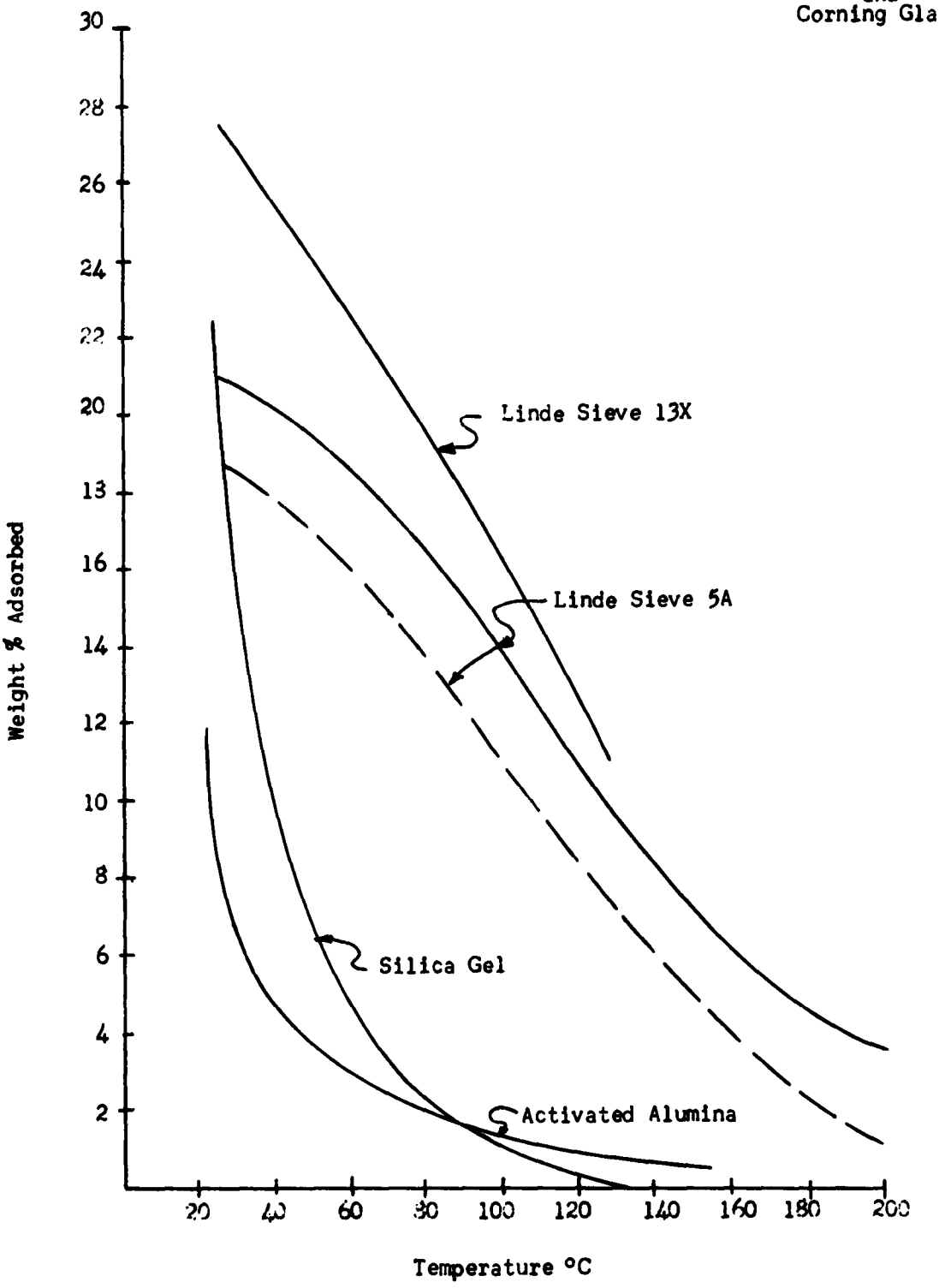
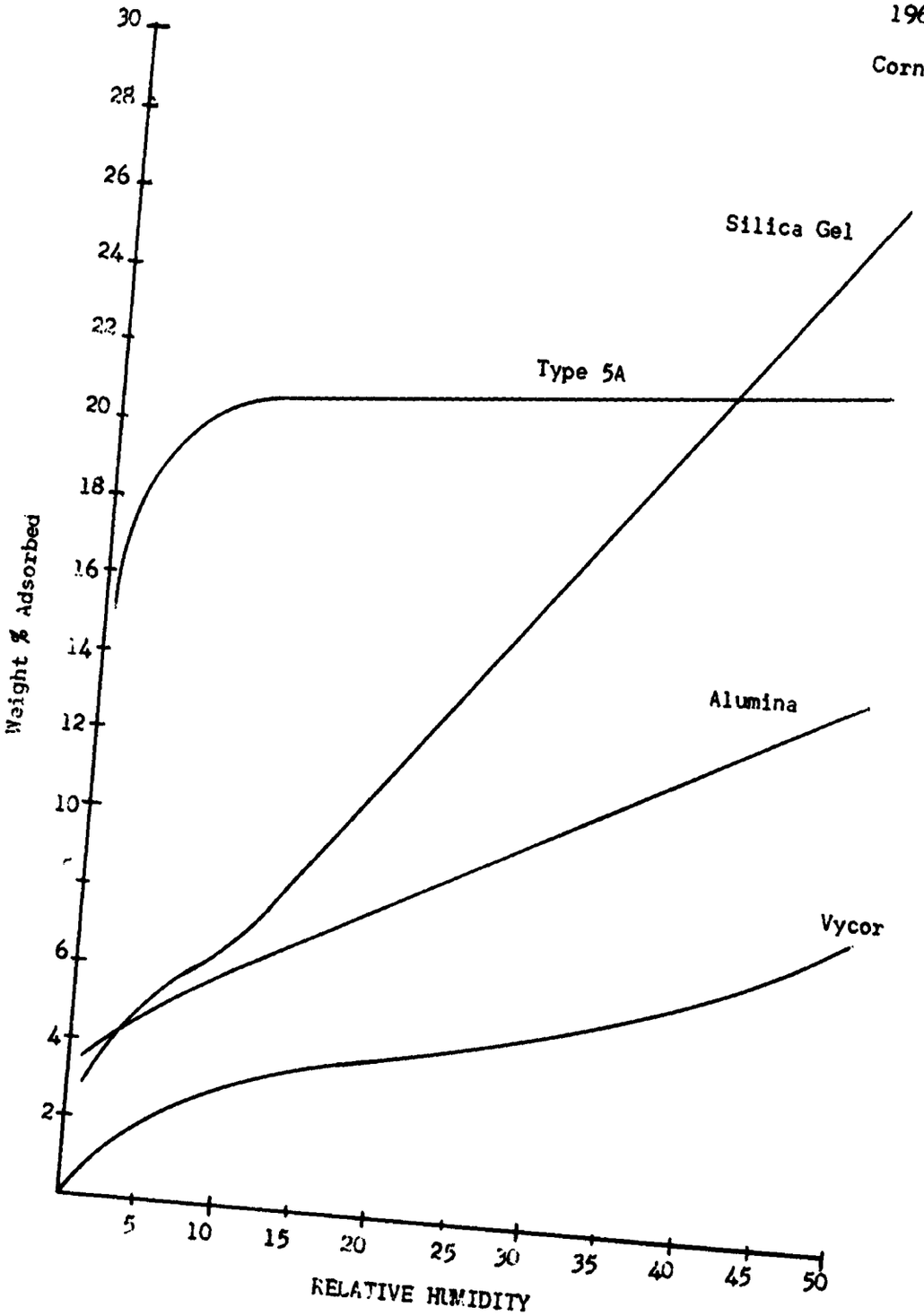


Fig. 3-4-Y

Ref: Molecular Sieves:
Charles K. Hersh
1961, p. 63
and
Corning Glass Works



Molecular sieves, in addition to water, adsorb CO_2, C_2H_2, NH_3, C_4, H_8, CO, C_2 H_6, C_2 H_4, H_2S, C_3 H_8, C_3 H_6, and SO_2.

It was previously indicated that activation must be performed but is not difficult. Activation is the process of moisture removal. Wallmark and Johnson [31] preheated molecular sieves at 200°C for 16 hours. At 250°C, Linde reported [37] that at 10 mm. Hg., the water in weight percent removing for 4A and 5A were 3.5 and 2.0, respectively.

It is interesting to note that loose 5A powder causes deterioration of devices due to abrasion, while 4A powder has been found more suitable. The abrasive nature of molecular sieves limits the usage of loose powder. Cracking, chipping, spalling, and other defects are generated when molecular sieve preforms are subjected to vibration and centrifuge testing.

Analysis of Getter Types - Thirsty Vycor. Thirsty vycor, a porous glass which is an intermediate in the manufacture of Corning Vycor brand glass ware, is essentially a finely divided amorphous silica with a consolidated instead of a loose powder structure. It exhibits exceptional mechanical strength. In addition, it has the advantages of cleanliness, freedom from ionizing impurities and organic contaminants, and closely controlled and reproducible manufacture. [38] The porosity, 29% is lower than the Linde molecular sieves. A typical composition of this getter is: 96.3% SiO_2, 2.9% B_2O_3, 0.7% R_2O_3 + RO_2 and 0.05% Na_2O.

[37] Linde Bulletin, F-8605B.
[38] M. Rand, J. of Elect. Soc., 109, 402 (1962)

In Figure 3-4-Z,[39] the weight percent of water pickup in porous vycor glass, previously activated at 200°C, is presented as a function of dew point and temperature.

Thus, the amount of moisture adsorbed by the vycor can be approximately determined for an encapsulated device as the temperature and encapsulating dew point are known.

The adsorption isotherms are shown in Figure 3-4-AA. The equation for the isotherm at low pressures may be written:

$$W = KP^{1/N} \qquad (3)$$

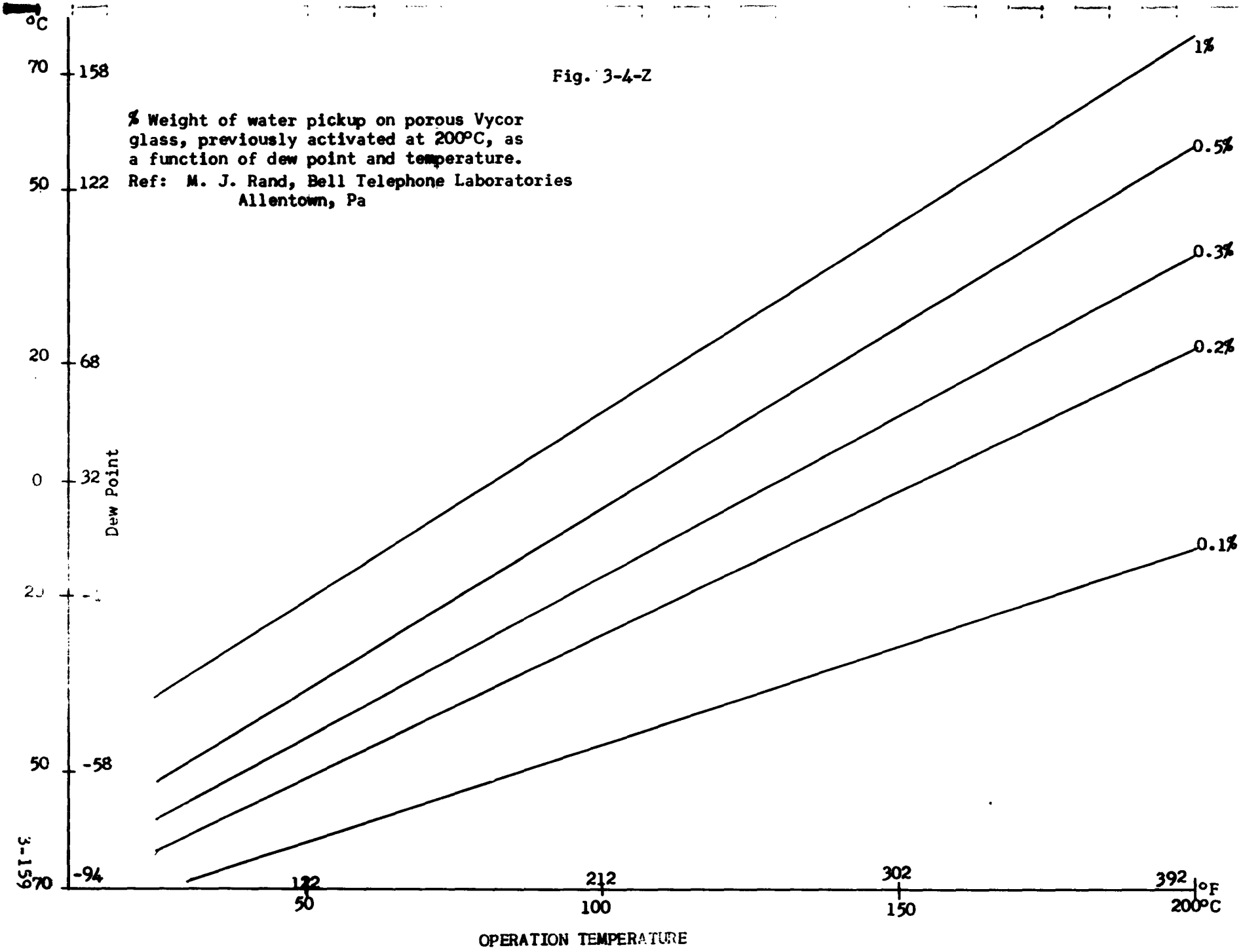
where W is the weight of water adsorbed
P is the partial pressure
K and N are constants

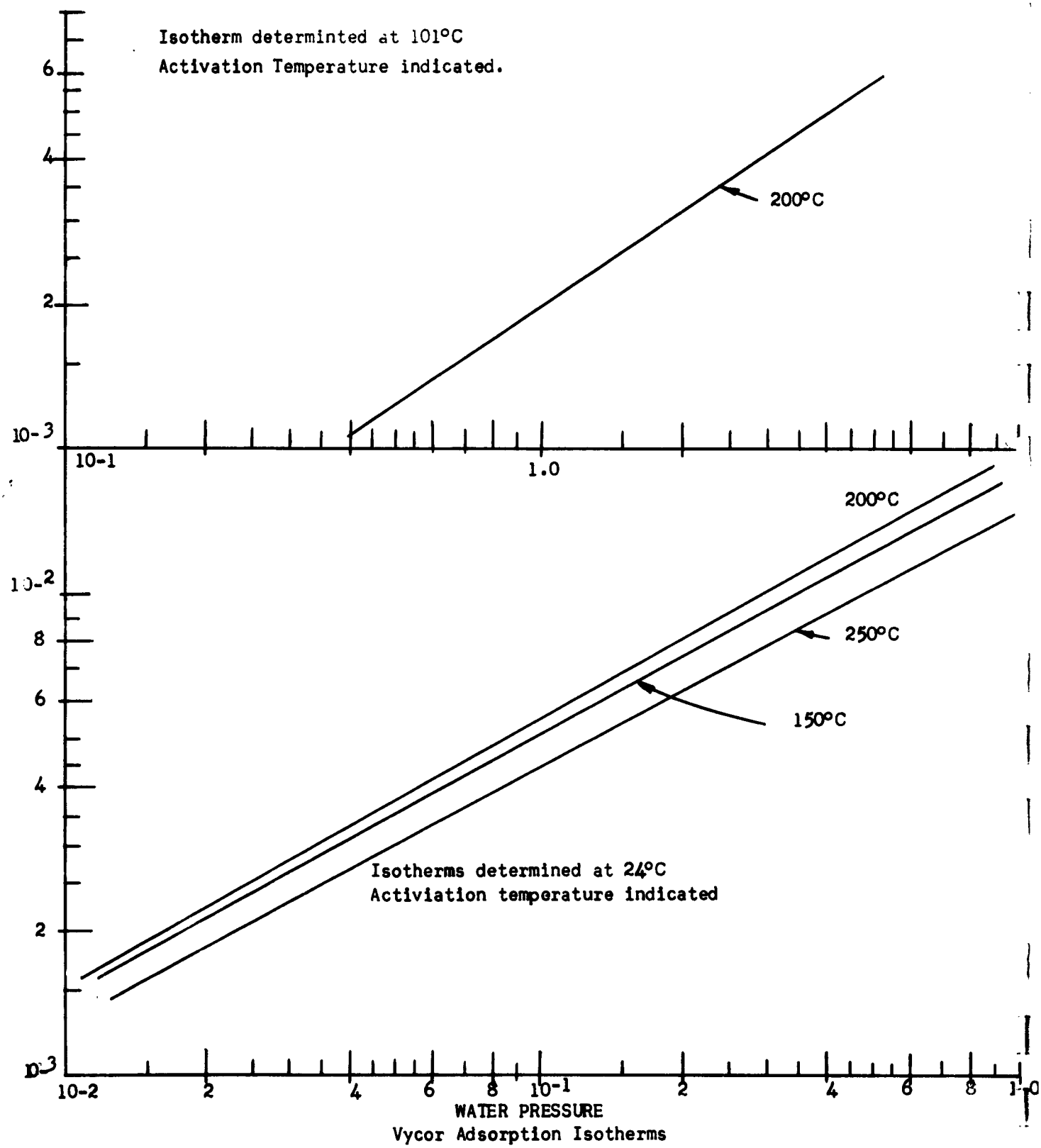
The activation of vycor used by Rand was a prebake at 200°C for 16 hours.[38] It has been reported by Corning that the water removal during activation will be generally completed within two hours, but the level is dependent mainly upon temperature.[39] Rand states, however, that there is no clearly definable point where the vycor will be completely "dry." There is a significant difference in activation efficiency between 200°C and 300°C. It has been concluded that the smaller pores begin to close at higher temperatures, thus causing loss in adsorptive capacity.[40] However, a 300°C, 30 minute dry nitrogen gas flush activation has been suggested as a practical semiconductor processing step. The most efficient activation procedure is vacuum baking at 200°C for 12 hours. Transistor stability with vycor has been achieved.

[39] I. Chapman, Corning Glass Works Report, L102, April, 1962.
[40] M. Nordberg, Corning Glass Works Report, L64, June, 1961.

Fig. 3-4-Z

% Weight of water pickup on porous Vycor glass, previously activated at 200°C, as a function of dew point and temperature.
Ref: M. J. Rand, Bell Telephone Laboratories
Allentown, Pa





Vycor Adsorption Isotherms

Fig. 3-4-AA

Getter Analysis - Barium Oxide. Barium has been used in electronic tubes, being the most active ingredient of flash getters.[32] Technical literature concerning the adsorption properties of barium oxide is sparse. However, as it is irreversible below 1000°C and because it is one of the most efficient dehydrating agents known,[40] it is practical to consider barium oxide for ambient control. Transistors with BaO exhibit very low gain.[41]

However, there are limitations to barium oxide's usage. Once the container is opened, the desiccant should be entirely consumed so that reactivation will not be necessary. The commercial availability is limited to powder and pellets, and may cause abrasive damage to the semiconductor. A light, loose powder is difficult to handle in a dry box through which high velocity dry air flows. It would be difficult to control the volume.

Chemical Oxidation of the Surface. Precap and vacuum baking and desiccants have produced stable transistors. Another approach is to chemically oxidize the surface. On units chemically oxidized, significant diode degradation resulted during 250 hour modulation life after 1000 hours at 135°C. The failure rate during storage life was 1.02%/1000 hours. Most of the experiments included were concerned with technique modifications in an attempt to obtain stability during operating life testing.

Chemical Cleaning of the Surface. The use of special solvents to remove residual metallic ions after etching and washing

[40] Bureau of Standards Journal of Research, Vol. 12 (1934)
[41] Ainich, J. A., Cullen, G., EGS, Indianapolis Meeting, Spring, 1961.

would lower the surface recombination sites. Thus, higher gain and a low diode saturation current would result. Technical literature concerning the use of boiling solvents has not been located. There is no available literature pertinent to the resultant device stability at elevated storage temperature and under operating life conditions.

Outline of Experiments. As the result of the treatments used, the surface recombination velocities varied considerably throughout the experiments. In most cases, accumulation layers were formed. As the collector diode degradation is the major failure mode and the treatments utilized significantly affected the gain level, units generally regarded as being out of the gain limits were not dropped. A more complete understanding of the results will be achieved by their inclusion.

The available data is summarized in Figures 3-4-BB and 3-4-CC. The first group is concerned with precap baking, vacuum baking, and chemical oxidation and cleaning. Devices with desiccants are included in the second group.

The theoretical discussion and justification of procedures have already been presented. Although VF_1 parameter is not included in the data, it was a criterion for rejection. 2 volt diode rejects and VF_1 rejects are included in the observed failure rate.

Experimental Procedure. These experiments are concerned with precap baking and chemical treatments of the surface to achieve stability.

2-1. Vacuum Bake at 135°C for 1 hour at 10 microns. Transistors were transported to the pilot line equipment after being etched and washed by production. The units were washed in methanol prior to placement in the oven. After reaching temperature, the devices were baked one hour under 10 microns. The units were then removed and capped as soon as possible. The dew point was -52°C. The caps were baked with the units.

2-2. Vacuum Bake at 135°C for 13 Hours at 10 Microns. Transistors from the same production group as those used in 2-1 were processed immediately after the removal from the oven. In this experiment, the units were processed identically as in 2-1, except that the time factor was 13 hours.

2-3. Vacuum Bake at 135°C for 1 Hours at 145 Microns. Transistors from the same production group as those used in 2-1 were processed at the same time as 2-1 in an adjacent oven. The same procedure outlined in 2-1 was used.

2-4. Vacuum Bake at 135°C for 13 Hours at 145 Microns. Transistors from the same production group as those used in 2-1 were processed at the same time as 2-2 in an adjacent vacuum oven. The same procedure as in 2-1 was used, except the time factor was 13 hours.

2-5. Precap Bake for 0.7 Hours at 130°C. The production units were baked for 0.7 hours at 130°C.

The ambient was dry air at approximately -40°C dew point flowing at approximately 20cfm. The transistors were cooled for 2 hours in dry air with a -40°C dew point, and then encapsulated by production.

2-6. Precap Bake for 1 Hour at 130°C. Production transistors from the same group as 2-5 were processed identically as 2-5, except that the precap baking period was 1 hour.

2-7. Pre-cap Bake for 1 Hour at 130°C, Capped "Hot." Production transistors from the same group as 2-5 were processed identically as 2-5, except that upon completion of the precap baking, the devices were transported hot through room ambient and capped by production within 20 minutes after removal from the heat.

2-8. Boiling Solvent "A." After standard production etching and washing, transistors from the same production group as 2-5 were transported in methanol, placed in boiling solvent "A" for 10 minutes, washed in methanol and transported to the production facility for a 15 minute precap bake after air drying. After cooling 2 hours in a controlled atmosphere, the devices were encapsulated by production.

2-9. Chemically Oxidized. Transistors from the same production group as 2-5 were chemically oxidized and baked for 1 hour as in 2-6.

2-10. Boiling Solvent "B." This experiment was the same as 2-8, except it was performed on a different day's production and that a different solvent was used. Also, the units were transported to the precap baking facility in methanol.

2-11. Chemically Oxidized - Modified Process. The transistors were processed from the same production lot as 2-10. The procedure was basically the same as 2-9, but the chemical solution was modified by the usage of methanol.

2-12. Boiling Solvent "C." Same as 2-10, except the solvent was different.

2-13. Boiling Solvent "D." Refer to 2-10. The solvent was different, however.

2-14. Chemically Oxidized - Boiling Solvent "B." Refer to 2-9. After the one hour bake, the units were placed in baking solvent "B." Refer to 2-10.

2-15. Vacuum Bake 2 Hours at 4×10^{-6} mm. Hg. at 135°C. Transistors were transported to the pilot line in deionized water after production etching and washing. They were washed in methanol and placed with washed caps in the vacuum oven. After the vacuum and temperature conditions were met, the devices were vacuum baked 2 hours at 135°C at 4×10^{-6} mm. Hg. The devices were capped, one at a time, to reduce moisture adsorption during cooling. The encapsulating ambient was -52°C dew point.

2-16. Repeat 2-1. It was found necessary to repeat 2-1 as there was evidence of localized overheating. Transistors were baked 1.25 hour at 25 minutes.

2-17. Vacuum Bake, 4 Hours at 4×10^{-6} mm. Hg. at 135°C. This experiment was performed as 2-15, except that the baking period was extended to 4 hours total. These units were from the same production group as 2-16.

2-18. Chelating Agent in the Chemical Oxidizing Agent. Triethanolamine was placed in the oxidizer and the devices were processed as per 2-9.

2-19. Vacuum Bake, 50 Microns at 135°C for 2 Hours. Production transistors were processed as in 2-15, except that the vacuum was only 50 microns.

2-20. Vacuum Bake, 90 Microns at 135°C for 2 Hours. Units from the same production group used in 2-19 were vacuum baked in the adjacent vacuum oven for 2 hours at 90 microns, and at 135°C. The devices were capped as in 2-15.

2-21. Chemically Oxidized and Rewashed. Refer to 2-9. After the one hour bake, all the transistors were rewashed, precap baked .25 hours, and encapsulated.

These experiments are concerned with the use of desiccants to achieve diode and gain stability.

3-1. Precap Baked, 1 Hour, Encapsulated with Thirsty Vycor. Production transistors were processed as in 2-7. Activated vycor preforms were placed on the base terminals just prior to encapsulation. The activation process consisted of an air bake at 235°C for 3.25 hours.

3-2. Chemically Oxidized and Encapsulated with Thirsty Vycor. Production units from the same group as 3-1 were chemically oxidized as in 2-9. Vycor preforms, activated as in 3-1, were placed on the base terminals.

3-3. Standard Production Encapsulated with Vycor. Production units from the same group as 3-1 were encapsulated with vycor activated per 3-1.

3-4. Standard Production Units Encapsulated with 5A Molecular Sieve. Production units from the same group as 3-1 were encapsulated with Type 5A Linde molecular sieve preforms. These preforms were activated as in 3-1. The preform dimensions were 0.250 diameter x 0.020 thick.

3-5. Vacuum Baked at 4×10^{-6} mm. Hg., and Encapsulated with Vycor. Production units from the same group as 2-15 were processed per 2-15. Activated vycor, 4 hours at 220°C, was placed in each device per 3-1.

3-6. Baked at 135°C for 0.75 Hour with Thirsty Vycor. Production transistors were transported to the

pilot facility and washed in methanol. Thirsty vycor saturated with water was placed on the transistors immediately prior to insertion into the oven. After a .75 hour bake, the devices were capped, one at a time, to reduce water adsorption. The caps were baked at the same time with the transistors. These units were from the same production group as 2-16.

3-7. Barium Oxide Encapsulated. Activated barium oxide powder, as obtained from the supplier, was placed on transistors just prior to encapsulation. The dew point was -47°C maximum.

Experimental Results.

Precap Baking.

a. When compared to transistors varnished or vacuum baked, precap baked units exhibited lower ICBO means.

b. The difference in IEBO means for the various experiments in Figure 3-4-BB may not be significant as the variations may be actually in the same production lots.

c. The 1 hour precap bake, experiment 2-6, has produced a relatively stable gain. But the diode current means at rated voltage are high. The gain shift for normal production, precap baked 0.75 hours,

Experiment No.	Experiment Description	ICBO After Cap	ICBO After Age	ICBO 2	ICBO 4	ICBO 6	ICBO A/C	ICBO A/A	IEBO 2	IEBO 4	IEBO 6	IEBO A/C	IEBO A/A	
2-1	10 Microns- 1 Hr. Bake	.74 (.45)	1.1 (.78)	.96 (.88)	.79 (.90)		.49 (.44)	.64 (.45)	.71 (.8)	.68 (.97)		154.2 (29.4)	166.8 (37.7)	20 (3
2-2	10 Micron- 13 Hr. Bake	.65 (.61)	1.48	.86 (.84)	.68 (.65)		.55 (.43)	.87	.67 (.46)	.64 (.42)		190.0 (27.3)	194.3 (43.2)	24 (4
2-3	Approx. 145 Mycrons 1 Hr. Bake	1.36 (.96)	1.72 (1.06)	1.38 (1.04)	1.64 (1.59)		.76 (.66)	.96 (.62)	.82 (.63)	.98 (1.01)		138.7 (20.8)	144.8 (24.6)	18 (3
2-4	Approx. 145 Mycrons 13 Hr. Bake	1.5 (.9)	2.4 (.96)	.89 (.62)	.74 (.57)		.25 (.23)	.37 (.34)	.36 (.4)	.35 (.32)		131.2 (28.0)	169.0 (39.5)	18 (4
2-5	3/4 Hour Air Bake	1.0 (.89)	1.6 (1.1)	1.5 (1.0)	1.86 (1.50)		.46 (.38)	.52 (45.0)	.51 (.42)	.54 (.51)		154.8 (21.0)	188.4 (20.6)	20 (2
2-6	1- Hour Air Bake	3.13 (5.6)	2.4 (1.26)	1.88 (1.1)	2.10 (1.26)		2.14 (5.8)	.92 (.87)	.83 (1.0)	1.01 (1.15)		179.3 (25.3)	196.4 (22.2)	20 (2
2-7	1 Hour Bake, Cap Hot	1.32 (1.1)	1.92 (1.1)	1.41 (1.0)	1.67 (1.48)		.76 (.75)	.62 (.72)	.58 (.73)	.50 (.62)		156.5 (19.8)	184.0 (27.7)	20 (2
2-8	Boiling Solvent "A"	1.80 (1.3)	1.57 (1.2)	1.50 (1.3)	1.87 (1.65)		.62 (.78)	.65 (.67)	.52 (.52)	.60 (.53)		172.9 (21.8)	190.7 (24.4)	21 (2
2-9	Chemically Oxidized 1 Hour Bake	1.17 (1.30)	.98 (1.1)	1.35 (1.3)	1.71 (1.96)		.58 (.59)	.69 (.65)	.69 (.63)	.74 (.68)		117.5 (23.6)	109.0 (18.5)	1((1
2-10	Boiling Solvent "B"	1.5 (1.04)	1.86 (1.28)	1.74 (1.42)			1.39 (1.05)	1.44 (1.04)	1.28 (.99)			141.4 (21.6)	117.3 (15.9)	1: (1
2-11	Chemical Oxidized Mod. Process	1.6 (.98)	1.79 (1.0)	1.90 (1.29)			3.93 (7.6)	1.43 (.75)	1.42 (.69)			125.0 (21.3)	117.2 (21.5)	1: (2
2-12	Boiling Solvent "C"	2.6 (1.50)	1.83 (.98)	1.51 (1.04)			1.17 (.45)	1.43 (.94)	.74 (.54)			101.2 (14.6)	112.0 (13.7)	1: (1
2-13	Boiling Solvent "D"	2.35 (1.78)	1.77 (1.23)	1.67 (1.28)			1.81 (4.75)	.85 (.54)	.72 (.53)			119.9 (13.6)	118.3 (11.6)	1: (2
2-14	Chemically Oxidized Boiling Solvent "B"	1.32 (.88)	1.63 (1.16)	2.10 (1.69)			1.24 (.84)	1.43 (.79)	1.70 (.87)			132.0 (20.4)	107.7 (18.6)	1((1
2-15	10^{-6} Vacuum Bake, 2 Hrs. 135°C	2.83 (1.0)	3.30 (.17)	6.73 (2.48)			.63 (.07)	.47 (.49)	.60 (.70)			265.3 (23.9)	265.7 (42.0)	2' (5
2-16	Rerun 2-1	2.45 (1.1)	2.42 (1.0)	2.0			.45 (.35)	.40 (.36)	.33			134.3 (34.7)	160.2 (31.5)	2:
2-17	10^{-6}, Hr. at 135°C	4.0	1.2	1.3			2.1	2.5	1.9			157.0	150.0	2(
2-18	Chelating agent in Oxidizer	2.0	>25.0				.6	>25.0						
2-19	50 Microns - 2 Hrs													
2-20	90 Microns - 2 Hrs													
2-21	Chemically Oxidized Rewash													

NOTE: ( ) - Standard deviation of parameter

2

	IB_2				2 Volt Diode						Failure Report			
6	A/C	A/A	2	4	6	A/C	A/A	2	4	6	Number Units After Age	Failures Determined in Nth Week 2	4	6	Failure Rate /1000 Hours
	154.2 (29.4)	166.8 (37.7)	204.1 (30.7)	190.0 (29.4)		102.3 (25.4)	77.0 (15.2)	75.5 (16.7)	79.4 (17.3)		15	0	0	0	6.7
	190.0 (27.3)	194.3 (43.2)	247.0 (44.1)	237.8 (35.4)		103.0 (24.2)	74.2 (19.4)	72.3 (12.6)	77.0 (13.5)		11	0	0	0	9.0
	138.7 (20.8)	144.8 (24.6)	185.4 (33.4)	172.2 (24.1)		83.1 (14.9)	45.1 (7.5)	44.0 (7.4)	54.8 (20.4)		16	0	0	0	6.2
	131.2 (28.0)	169.0 (39.5)	187.9 (40.0)	177.6 (37.4)		72.9 (9.6)	58.2 (19.2)	47.9 (17.2)	50.1 (14.1)		8	0	0	0	N/A
	154.8 (21.0)	188.4 (20.6)	204.8 (25.0)	209.1 (26.1)		125.3 (188.7)	88.9 (15.0)	87.6 (14.2)	98.2 (16.2)		19	0	0		
	179.3 (25.3)	196.4 (22.2)	205.4 (28.1)	209.1 (28.3)		105.2 (80.0)	83.5 (16.5)	86.2 (17.1)	96.4 (19.1)		19	0	0		
	156.5 (19.8)	184.0 (27.7)	207.9 (25.4)	206.9 (25.2)		101.0 (75.8)	90.6 (29.4)	84.5 (21.7)	85.8 (29.0)		19	0	0		
	172.9 (21.8)	190.7 (24.4)	212.0 (28.0)	211.0 (25.9)		88.9 (12.4)	94.2 (15.4)	90.6 (13.8)	100.0 (15.4)		21	0	0		
	117.5 (23.6)	109.0 (18.5)	104.8 (17.9)	111.0 (19.2)		65.4 (8.4)	41.2 (21.6)	49.7 (21.5)	60.9 (19.7)		27	0	0		
	141.4 (21.6)	117.3 (15.9)	126.4 (17.0)			68.6 (10.4)	44.2 (9.3)	57.6 (14.7)			16	0			
	125.0 (21.3)	117.2 (21.5)	128.0 (28.3)			69.4 (25.1)	52.1 (20.3)	76.1 (21.5)			10	0			
	101.2 (14.6)	112.0 (13.7)	127.9 (15.7)			51.0 (8.6)	42.5 (8.2)	74.0 (15.2)			19	0			
	119.9 (13.6)	118.3 (11.6)	121.0 (24.9)			71.7 (7.6)	43.1 (7.7)	66.9 (17.2)			20	0			
	132.0 (20.4)	107.7 (18.6)	109.6 (18.6)			80.0 (19.2)	46.4 (10.6)	61.3 (13.2)			20	0			
	265.3 (23.9)	265.7 (42.0)	279.3 (53.7)			120.3 (23.5)	124.7 (9.5)	197.7 (41.4)			3	1 2V			
	134.3 (34.7)	160.2 (31.5)	228.5			110.7 (133.3)	61.0 (12.0)	107.0			0	0			
	157.0	150.0	206.0			590.0	87.0	138.0			1	0			
						76.0					0				
											12				
											4				
											34				

FIGURE 3-4-BB

Experiment No.	Experiment Description	After Cap	After Age	ICBO 2	4	6	A/C	A/A	IEBO 2	4	6	A/C	A/A
3-1	1 Hour Bake plus Vycor	1.9 (1.2)	2.0 (.9)	1.68 (.85)			1.0 (.7)	1.0 (.77)	1.64 (1.5)			156.7 (27.1)	189.1 (31.7)
3-2	Chemically Oxidized plus Vycor	1.45 (.9)	1.90 (1.6)	1.90 (1.13)			.8 (.88)	.94 (.89)	.99 (.85)			117.9 (24.0)	97.2 (16.6)
3-3	Regular production plus Vycor	1.45 (.9)	1.89 (1.1)	1.67 (1.04)			1.1 (1.4)	.9 (.9)	.98 1.17			94.5 (13.3)	191.2 (25.7)
3-4	Regular production plug 5A	1.56 (.87)	1.42 (.89)	2.54 (4.26)			.87 (.64)	.89 (.73)	.83 (.66)			189.0 (35.1)	195.4 (21.4)
3-5	10^{-6} Bake 1 Hour with Vycor	1.51 (1.0)	3.25 (.55)				.30 (.05)	1.78 (.52)				236.5 (27.7)	229.0 (23.7)
3-6	Baked W/Vycor 1 Hr. at 135°C	3.48 (3.7)	2.75 (1.26)				.21 (.13)	2.23 (.85)				148.4 (14.3)	213.7 (18.0)
3-7	Barium Oxide												

NOTE: ( ) - Standard deviation of parameter

2

	IB_2					2 Volt		Diode			Number Units After Age	Failure Report Failures Determined in Nth Week			Failure Rate /1000 Hours
6	A/C	A/A	2	4	6	A/C	A/A	2	4			2	4	6	
	156.7 (27.1)	189.1 (31.7)	174.3 (43A)			97.6 (19.7)	92.1 (13.8)	146.7			22	0	0		
	117.9 (24.0)	97.2 (16.6)	101.2 (24.7)			77.0 (11.0)	49.4 (7.9)	6.5 (13.6)			20	0	0		
	94.5 (13.3)	191.2 (25.7)	188.7 (31.4)			66.5 (28.8)	82.2 (30.9)	126.0 (26.8)			26	0	0		
	189.0 (35.1)	195.4 (21.4)	186.8 (34.0)			111.7 (23.9)	53.6 (12.7)	84.3 (18.3)			24	1 Icbo	0		
	236.5 (27.7)	229.0 (23.7)				179.5 20.1)	161.5 30.8)				4	1 Icbo			
	148.4 (14.3)	213.7 (18.0)				88.0 (10.3)	125.5 (14.3)				4	0			

FIGURE 3-4- CC

and precap baked one hour, are 45%, 22%, and 9.5%, respectively. The diodes for the three precap baked experiments remained stable during storage. No diode failures have occurred yet.

d. Chemically oxidized units exhibit high and stable gain, as well as high diode current means. Normally, the two volt diode characteristic is lower than standard production. No rejects have been generated to date.

e. Triethanolamine as a chelating agent in the chemical oxidizer caused rapid degradation. The after age diode means were in excess of 25ma at the rated voltage as compared to a specification limit of 4ma.

f. The general effect of hot solvents was to produce a high gain, stable transistor according to the available data. One indication of a cleaner surface is that the 2 volt collector diode means are very low. The lower gain using hot solvent "A" may be due to either the efficiency of the solvent or due to the room temperature air dry used prior to precap baking. Further investigations are planned. No rejects have been generated to date. Recent results for another transistor type using solvent "B" indicated that the diode degradation during modulation life testing was significantly lower than for units chemically oxidized.

Dessicants:

a. As is the case for most of the experiments, these

groups have not completed the 1000 hour storage test.

b. The parameters, particularly gain, of chemical oxidized transistors were not affected by the desiccant.

c. Standard production units and devices precap baked one hour attained the same gain level after aging.

d. Transistors baked one hour, transported to the encapsulation chamber and sealed with a desiccant exhibited the same initial gain level and the same relative gain shift as units processed identically, but without desiccant - (Experiments 3-1 and 2-7). Their diode characteristics are similar.

e. Data pertaining to the use of barium oxide has not been evaluated.

f. No difference in gain was noted using either 5Å or vycor.

g. Vycor ring preforms, both loose on the base terminals or held by "Tinnerman type nuts," did not spall or break during cumulative low and high frequency vibration and shock tests.

Vacuum Bake.

a. There is evidence that there may be localized overheating during vacuum baking. Solder splashes

have been found on the collector junction and collector side of the wafer. Although attempts have been made to further correct the vacuum oven, results have not eliminated the problem. Acceptable transistors have been generated, but the sample sizes do not facilitate failure rate measurements.

b. A white residue was detected on the collector surface after aging on units from Experiment 2-20. The oven used was only used for 2-3, 2-4, and 2-20. Samples have been sent for spectrographic analysis of the deposit. Solder splashes were not observed.

c. For the limited data from 2-1 and 2-2, it appears that an hour vacuum bake does not produce a device with stable gain. The gain significantly decreased during aging.

d. Possibly the vacuum bake at 10 microns was more efficient in moisture removal. Lack of gain stability was observed for units baked at 145 microns for 1 hour and 13 hours.

e. Experiment 2-15 was an extension of the vacuum bake period used in 2-1. Although the oven was adjusted in an attempt to reduce solder "splash," only three acceptable units were obtained. These units exhibited very low and stable gain, suggesting that future experiments should utilize a longer bake cycle under very high vacuum.

f. Solder splashes were present on units baked two hours at 50 minutes. Minor modifications are still necessary to reduce this rejection mode.

g. For transistors vacuum baked and encapsulated with desiccants (3-5 and 3-6), the results were the same as above; i. e., very limited units due to solder splash were available for evaluation.

h. Photographs 3-4-DD and 3-4-EE show solder on the collector side of the wafer. The solder exhibits a dendritic structure that appears to be indium, and is not found on the emitter side after bake.

Conclusions. Precap baking for one hour, chemical oxidation, varnishes, desiccants and boiling solvents all improve reliability according to the available data. Modulation life test data is now being compiled on experimental devices which have passed 1000 hour storage testing. Larger groups are to be processed on the basis of the combined data and these units will be submitted for approval.

As a result of solder splashes on the collector diode, additional experiments are necessary to properly evaluate vacuum baked transistors. Acceptable devices have exhibited gain sensitivity as expected. This is due to the encapsulated ambient and nature of the established oxide. The effects of moisture as reported by Wahl have also been duplicated.

Definite conclusions can not be presented in this report as data is still being obtained.

Fig. 3-4-DD

Demounted element exhibiting solder splash on the collector side.

Fig. 3-4-EE

The same element as above magnified to approximately 50X to show the structure of solder splash.

Program for the Next Quarter. The analysis of the experimental data is nearing completion. During the next quarter, the results in Paragraph 3.4.6 will be combined with desiccant experiments in an attempt to arrive at the stability given by desiccants and maintain the higher gain resulting from improved cleaning and/or coating.

3.4.8 Contamination Studies - R. M. Matuska, R. P. Anjard.

General and Engineering Status. To purposely contaminate at low concentration levels, it is necessary to insure that a minimum of contaminants are generated from the sample itself. Considering the coefficient of expansion and particularly the electromotive force series, it was decided to generate ideal elements and ideal transistors. For these, then, the contaminants from the source would be reduced as much as possible.

There are two portions to the problem: reduce contamination from the element itself, and from the other integral parts - such as the mounting base, base ring, and solders.

Regarding the element, it was decided to alloy using pure indium. The standard base ring and solder would be replaced by tin plated molybdenum. By etching before mounting, the only metallic ions could be: germanium, indium, molybdenum, and tin. Although silver plated base rings would be attacked less by the etch, serious alloy difficulities were encountered. Serious limitations are also present in the use of molybdenum, even for experimental purposes. It was impossible to punch molybdenum base rings because of the metal hardness and stock feeding limitations. Photoetch techniques were developed to produce the

base rings from 5 mil sheets. The first samples are now being plated. However, plating to the molybdenum is difficult. It would be desirable to have antimony in the plating to obtain higher diodes and other characteristics. But the plater has advised that he can not plate 95% Sn - 5% Sb on our parts.

Because of the limitations with molybdenum, nickel base rings were consided although the coefficient of expansion is approximately twice that of germanium. Transistor elements have been alloyed using tin plated nickel base rings, and all of them were craked during alloying.

Quotations have been solicited for molybdenum base rings, plated and unplated; but information has not been received yet. As soon as 250 "proper" base rings are available, the "ideal elements" will be alloyed and then etched.

Program for the Next Quarter. These elements will be mounted in special fixtures and then etched in contaminated electrolyte. An uncontaminated control group will be run. The electrolyte will be contaminated with copper, iron, and lead ions. The group which will be etched in copper contaminated electrolyte will then be split into two groups, and, one of these groups will be treated with a boiling solvent.

The etching will be done in a small, closed, system to eliminate cross-contamination between the contaminated electrolytes. A etch control system is being assembled to duplicate the etching cycle that is used in the manufacturing area.

After etching and washing, the elements will be baked for one hour at 130°C. After baking, the elements will be placed on

special bases which have been baked for several hours at 150°C. These bases have been modified so that a wire extends upward from the pedestal. It is intended for this wire to penetrate the collector solder when the element is attached. The internal electrical connections will be made without soldering the leads. The standard emitter connector will be used and it will be held in place by spring tension. A "Tinnerman" type nut will lock the emitter connector in place. Likewise, the base rings will be held rigid by these nuts. The assembled devices will be capped hot to reduce adsorption. Before capping, the caps will be baked for several hours at 200°C, and, during capping, the dew point in the encapsulation chamber will be held below -47°C.

Diode measurements will be made on the finished devices to determine if any significant differences can be detected in diode degradation.

3.4.9 Other Advanced Techniques - M. E. Stanton.

General and Engineering Status. Samples have been submitted to the manufacturer of a solid source mass spectrometer for a demonstration analysis. The samples were prepared to show the capability of the instrument to analyze for both surface and bulk impurities.

The Battelle study showed a possible application of microchemistry techniques to film analysis on transistors. These tests have been attempted in our lab, but the microscope illuminator available is not the most suitable for the study of films on a highly reflecting surface. A dark field illuminator will be investigated in the next quarter in an attempt to improve the observation of film contaminates and the microchemical study of these films.

DELCO RADIO

4.0 IDENTIFICATION OF PERSONNEL

4.1 Personnel Changes.

Technical personnel, not previously identified, who actively participated in the program during the second quarter were:

J. M. Myer
J. F. Norwich
C. E. Wampole
R. J. Ropes
F. E. Townsend
G. H. Gould
Z. L. Fordyce

4.2 Engineering Time.

From August 1, 1962, through October 31, 1962, there were 6,236 hours spent by Delco Radio personnel on the engineering efforts toward fulfilling the contract commitments.

4.3 Personnel Biographies.

Personnel biographies not included in the proposal or previous report are included in this report on the following pages.

John M. Myer - (B.S. Chemistry, Indiana University) - Senior Process Engineer.

Mr. Myer joined Delco Radio as a process engineer in 1953. From 1953 to 1960, Mr. Myer was a chemist in the finishing section of radio process engineering.

In 1960, Mr. Myer was transferred to the chemical area of semiconductor process becoming section head of the Chemical and Metallurgy area in 1961.

In 1962, Mr. Myer was transferred to section head of the project engineering - semiconductors of the process department.

Prior to joining Delco, Mr. Myer taught chemistry in Kokomo High School for two years.

John F. Norwich (B. A., Chemistry, St. Anselm's College, Manchester, N. H.) - Process Engineer.

Mr. Norwich joined Delco Radio in 1961, and has been employed as a process engineer. He has been associated in semiconductor manufacturing since 1956. As an engineering manager at General Instrument Corp., Rhode Island, his prime responsibilities were reliability of devices and process techniques used in fabrication of NPN germanium devices.

C. E. Wampole - (B. S. and M. A. Degrees with graduate study toward a Ph. D., Ball State and Indiana Universities) - Senior Project Engineer - Device Chemistry, Research and Advanced Development - Semiconductors Section.

Mr. Wampole's present position is that of Senior Project Engineer responsible for Device Chemistry in the development of semiconductors.

As such, his duties are to analyze, investigate and develop new processes suitable for future production, and to prescribe, supervise, and coordinate routine and special chemical analyses.

In 1951, Mr. Wampole was employed as a chemist at Delco Battery - GMC, where he analyzed and released materials to production; and ran wet chemical and spectrographic analysis for control and research. From 1952 to 1956, he served as head of chemistry and physics, and Director of Audio Visual Aids at Central High School, Fort Wayne, Indiana. Joining the Magnavox Company, Mr. Wampole became the plant chemist for the newly constructed facility at Urbana, Illinois. He organized the new plant's printed circuit department and set up the electroplating section, including the control laboratory. As they were staffed, he remained in a supervisory capacity. In the performance of his duties, Mr. Wampole provided a wide range of services within the fields of physical chemistry and electrochemical research in support of engineering and production. This included familiarity with chemical

problems associated with radar, electromagnetic devices, missile components, A. S. W., and ordnance fuzing. He established a systematized method for chemical procedures and was responsible for the compliance to military specifications of all plating and finishes. While with Bendix Company (A. E. C.), in the capacity of senior process engineer, he supervised process engineering in printed circuit fabrication. Among the processes he developed were printed circuit cables and plated-thru-holes techniques. In September, 1959, Mr. Wampole joined Delco Radio.

R. J. Ropes - (Certificate, Radio Engineering, Capitol Radio Engineering Institute; Diploma, Indiana Business College; Undergraduate work at DePauw University, University of Iowa, Indiana University Center and Purdue Extension. Specialized courses in Statistics at Indiana University Center, General Motors Institute and Purdue University; U. S. Naval Aviation WWII) General Foreman, Quality Control Department - Semiconductors.

For the past two years, Mr. Ropes has been responsible for the Quality Control function involving all transistor manufacturing and testing, as well as the design, establishment and implementing of the various Quality Control plans for this area. Prior to the above assignment, Mr. Ropes' job responsibilities involved eight years as a Foreman, Quality Control Department, involving both Military (T-38 Skysweeper, A-4 Gunsight Amplifier), and Semiconductor Department and Commercial projects and ten years in Test Engineering Construction and Design. During the recent Reliability Improvement Program on Minuteman Transistors, Mr. Ropes was responsible for the quality control function in the performance of this contract.

He is author of the article "High Stability Oscillator," Radio & Television News, June, 1957. He is a member of the Amercian Society for Quality Control.

F. E. Townsend - (Indiana University)- Quality Control Foreman.

Mr. Townsend has attended Indiana University Center and is a graduate of U. S. Naval Communication's School. He served 4 years in the U. S. Navy during the Korean Conflict.

His work experience includes 1 year as Electronic Technician, Civil Service (Shipyard), and 8 years as a Test Designer, Test Engineering, Delco Radio.

For the past two years, Mr. Townsend has had the responsibility of supervising the Environmental test area, Semiconductor Quality Control, and is continuing in this area.

J. H. Gould - Lab Technician, Research and Advanced Development - Semiconductors.

Prior to joing Delco Radio, Mr. Gould served in the U. S. Air Force. During this time, he received special training in radar and electronics.

Mr. Gould joined Delco Radio in March of 1960, as a lab aide. He has developed the cold etch techniques that have made the photographic etching of silicon and high accuracy electro-etching of molybdenum possible. He has also developed various plating solutions for use in the Chem. Lab. One of which is an electroless nickel bath that provides ohmic contact to P and N type germanium, and another electroless nickel that plates to highly diffused silicon where the standard solution fails.

Zed. L. Fordyce - Special Tester - Research and Advanced Development - Semiconductors.

Mr. Fordyce's responsibility is to assist in the analytical surface study program for the detection of contaminants.

Prior to joining Delco Radio Division, he served as an electronic technician with General Dynamics Corporation for four years. His duties were instrumentation of test B-58 Bombers and checkout of electronic subsystems for Atlas Missiles. Mr. Fordyce is a gruadate of DeVry Technical Institute in Chicago and has served in the U. S. Army as a Field Radio Repairman.